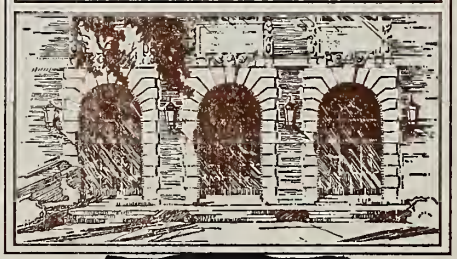


 UIUCDCS-R-75-715

NORMAN
(NORMalizing ANalyzer)

by

GARLAN JAY HUBERTS

April 1975

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

UIUCDCS-R-75-715

NORMAN
(NORMalizing ANalyzer)

BY

GARLAN JAY HUBERTS

April 1975

Department of Computer Science
University of Illinois
Urbana, Illinois 61801

This work was supported in part by Contract No. N000-14-67-A-0305-0024 and was submitted in partial fulfillment of the requirements for the degree of Master of Science in Computer Science, at the University of Illinois.

ACKNOWLEDGEMENT

The author is especially pleased to thank his advisor, Professor W. J. Poppelbaum. for the original proposal and for his advice and ideas that led to NORMAN becoming a reality.

The author would also like to thank the other graduate students working in the Information Engineering Laboratory under Professor Poppelbaum for their friendship, advice and constructive criticism.

Many thanks must also go to the Electronic Fabrication Group under the direction of Mr. Frank Serio for their many hours of work on the machine. They were responsible for laying out and building all of the printed circuit cards and doing much of the tedious job of wirewrapping. They also had the patience to check each wirewrapped connection they made.

The author would finally like to express his gratitude to Ms. Evelyn Huxhold for typing this thesis and to the drafting group who prepared the drawings.

TABLE OF CONTENTS

Page

LIST OF FIGURES

1.0 INTRODUCTION

The purpose of NORMAN as proposed by Professor Poppelbaum is to recognize two-dimensional figures under conditions of translation, rotation, and magnification by using an "intelligent input array" and probabilistic processing. The power of NORMAN is that the machine does not require any preconceived notions regarding the figures: they can be any arbitrary figure. Letters, numbers, or geometrical figures are all automatically normalized with respect to where they are placed over an array of phototransistors, the angular placement of the figure over the array, and also with respect to the size of the figure. A set of figures is stored by simply laying each figure over the array and pushing a button on the front panel. The machine stores the figures as normalized profiles. It can then be asked to recognize a figure and if a profile in its memory comes close enough to the profile of the figure laying on the phototransistor array, it outputs the fact that it has recognized that figure.

The first part of this thesis describes the phototransistor array and the circuitry immediately following it which provides the profile of the figure to the rest of the machine. The next part of the thesis describes the processing required to normalize the figure with respect to the three permutations. The final part is a more detailed board by board description of NORMAN followed by a short conclusion.

2.0 INPUT ARRAY

NORMAN uses a large array of phototransistors to "see" the figures it has to recognize. The phototransistors are mounted in holes drilled in a 1/2 inch thick piece of plexiglass painted flat black. The emitter and collector leads of the phototransistors are soldered to a large printed circuit board mounted on the underside of the plexiglass panel. The collectors are all tied to a positive 12 volts and the emitters are each brought out to connectors at the edges of the printed circuit board. An input figure which consists of a black figure on a transparent plastic sheet is laid on top of the phototransistor board and the black figure blocks off light to the phototransistors below it, while the others in the array are driven into saturation by four sixty watt light bulbs mounted about 18 inches above the board.

Figure 2.1 shows the shape of the input array of phototransistors where each small circle represents a phototransistor. While this shape may seem a little strange, it is quite logically derived. Figure 2.2 shows what is termed a "basic input array." Taking direction 1 as an example, current is summed by the amplifier circuit of Figure 2.3 for each one of the eleven lines in this direction. Note that because of the hexagonal symmetry of this array, direction 7 and direction 13 each have eleven lines where the spacing is identical to that of direction 1. Therefore each basic array has three sets of eleven lines, all sixty degrees apart from each other. If six sets of these basic arrays are overlayed with ten degrees difference between each and some simplifying approximations are made in the positions of a few phototransistors, the total input array shown in Figure 2.1 is obtained. Note that there is now a set of eleven lines every ten degrees

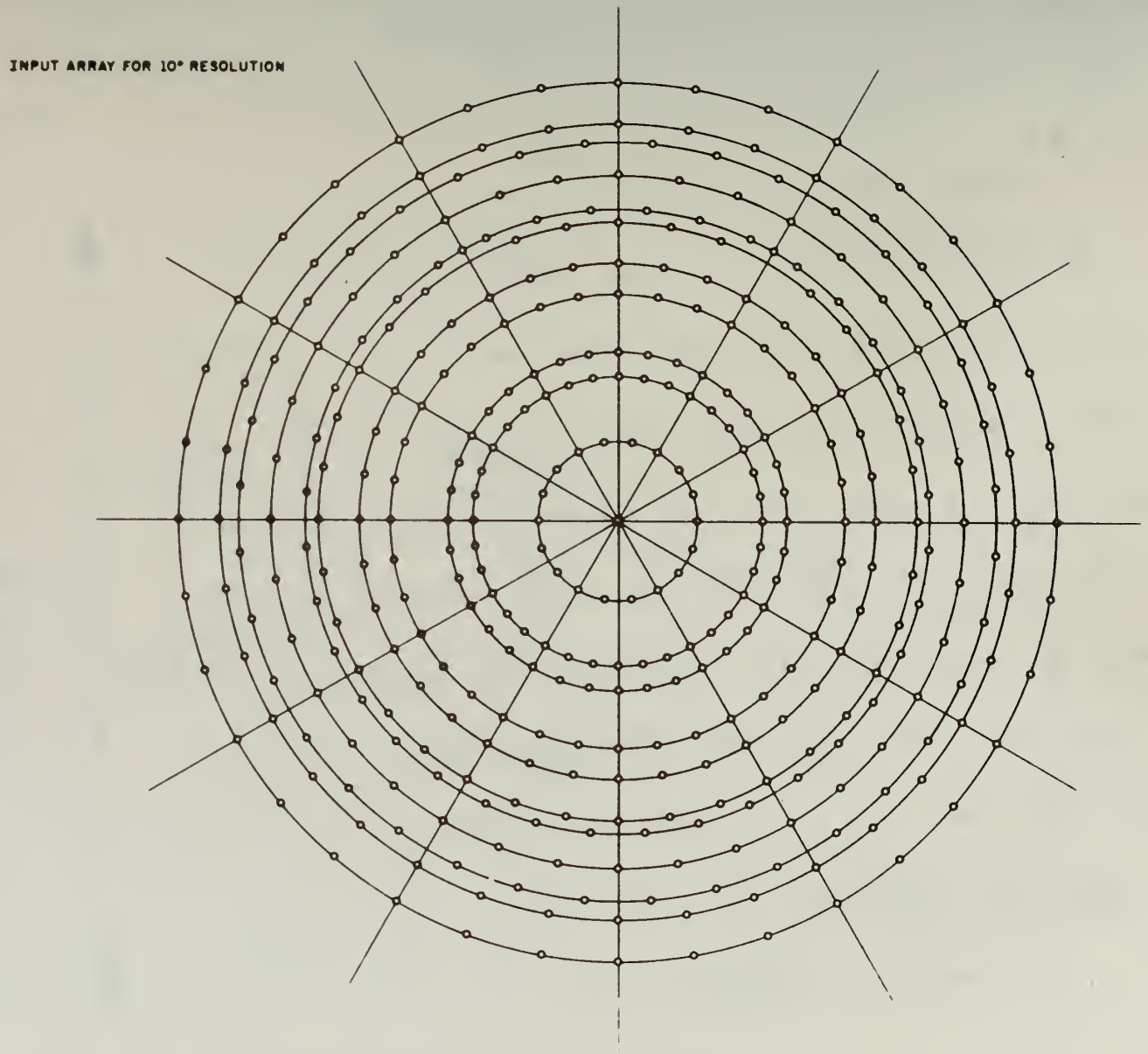


Figure 2.1 Total Input Array

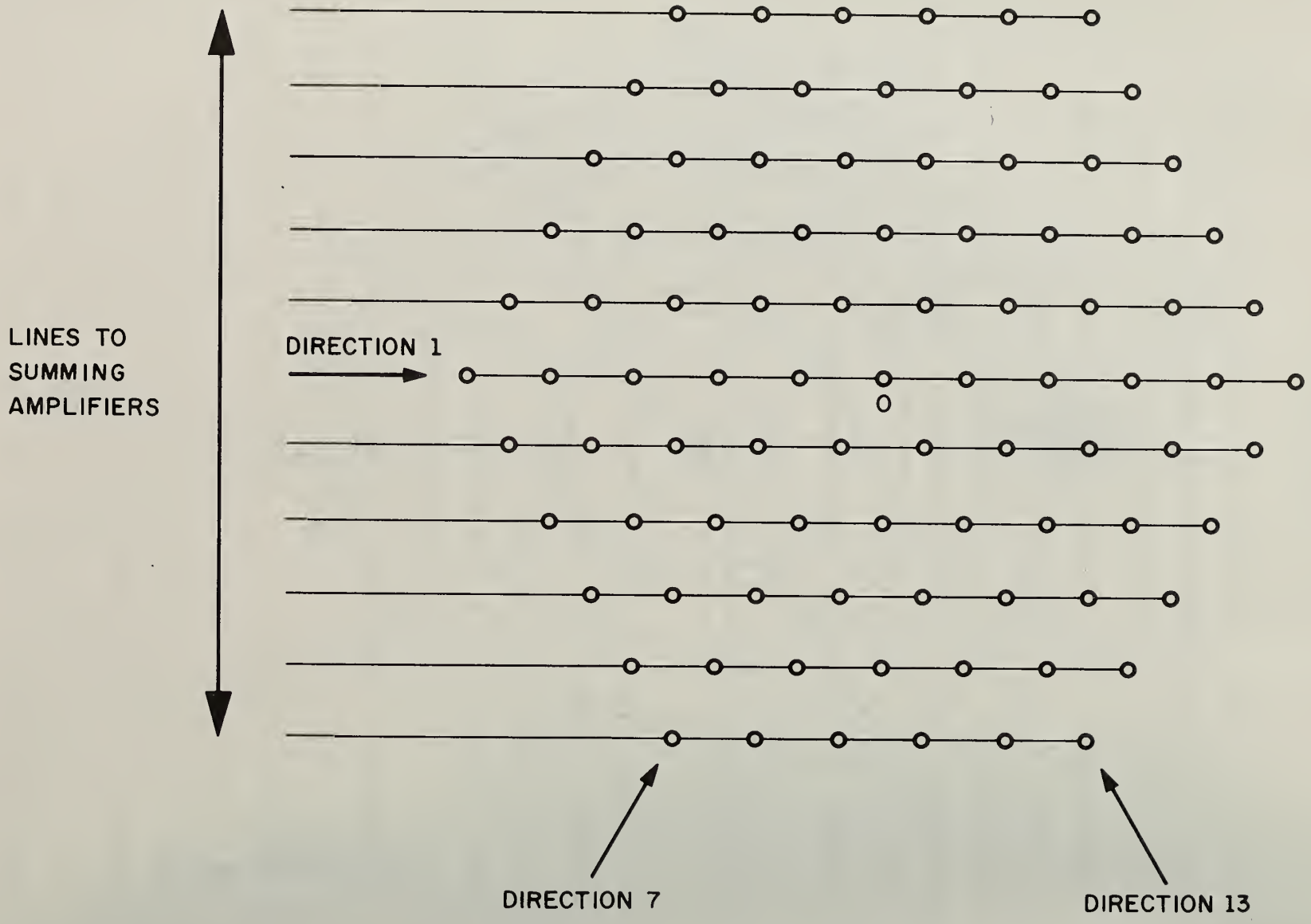


Figure 2.2 Basic Input Array

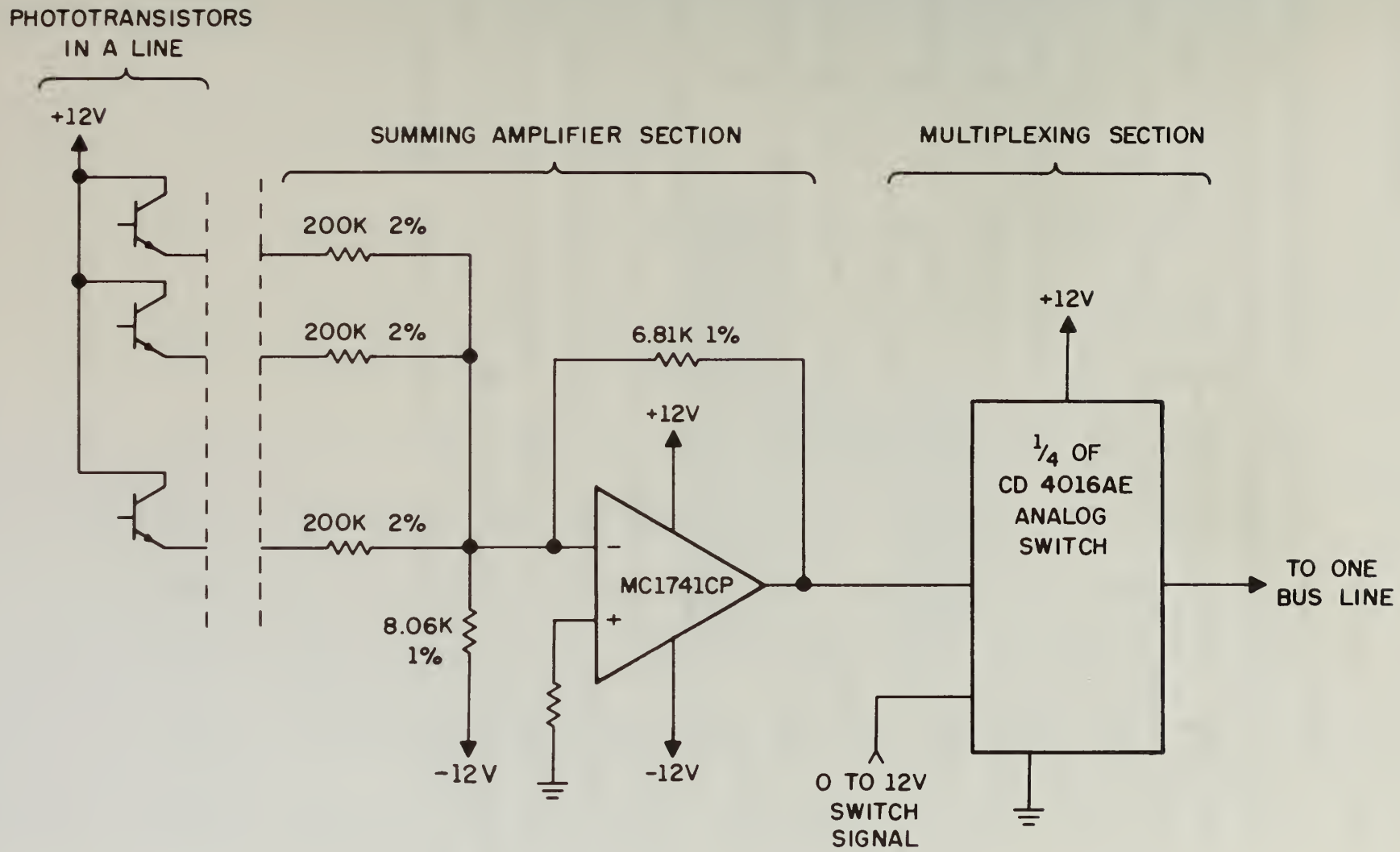


Figure 2.3 Summing Amplifier and Multiplexer

thereby providing ten degrees of rotational resolution for any opaque object placed over this array.

Referring back to Figure 2.3, the MC1741CP operational amplifier circuit does current summing from all the phototransistors in a line of the basic array. Each array then requires eleven op amps and results in eleven analog voltages. Each op amp is biased so that when all phototransistors in its line (varying from six to eleven) are saturated, the output voltage is 1.2 volts. The gain is set so that a change of 0.8 volts is seen every time a transistor is covered by a portion of the figure. Referring to Figure 2.4, it is easy to see that by summing currents along lines of phototransistors, positional information of the figure along these lines is lost. The voltages at the outputs of the op amps can be said to represent the "profile" of the figure since they are representative of only the width of the figure along those lines.

The machine has eighteen Input Boards which each contain eleven op amps and three CD4016AE integrated circuits. Each integrated circuit acts as a four channel analog switch. This arrangement enables NORMAN to send a switch signal to one of the eighteen Input Boards at a time to obtain one angular view of the figure. This profile is then digitized by an A/D Board and stored in a shift register on a board called the Analyzer Board.

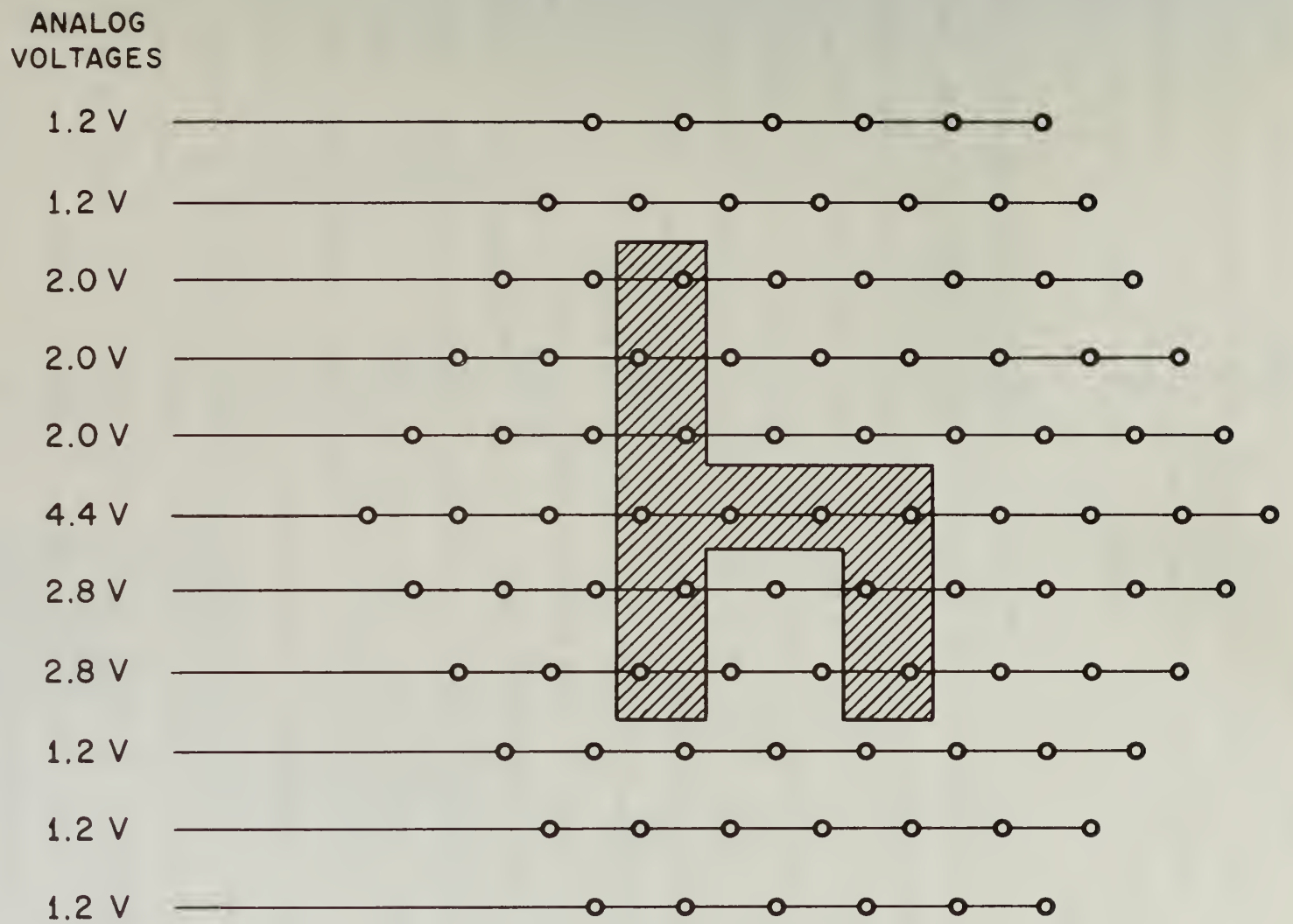


Figure 2.4 Profile Representation of Figures

3.0 NORMALIZING PROCESSING

Figures 3.1 and 3.2 show a block diagram of the system. Everything in Figure 3.1 except the bus analyzer has been previously discussed. After the eleven analog voltages representing the profile of the figure have been digitized and stored in the buffer, the bus analyzer takes over and does two things.

First it shifts each four bit number up from one register of the buffer to the next until the top register no longer contains the number "zero." The normal case for an input is shown in Figure 3.3. where an input figure, a triangle, is placed somewhere on the array. The lines of phototransistors not covered by the triangle have the number "zero" in their respective registers. This shifting action has the effect, to the rest of the machine, of moving the input figure up to the top edge of the array. This action removes all positional dependence for recognition of figures.

Secondly the bus analyzer starts with phototransistor line eleven and counts down from eleven until it hits the first non-zero line. The counter then contains the number of phototransistor lines covered by the input figure (termed "active" lines). This number indicates the size of the figure.

Referring to Figure 3.2, a time division distributor then samples two adjacent registers of the buffer and these numbers are converted into two synchronous random pulse sequences (hereafter referred to as an SRPS). Also converted into an SRPS is the number of active lines information from the bus analyzer. The nature of these SRPS signals is explained more fully in Chapter 4 under Section 4.5, suffice it here to say that they are digital pulse signals which when integrated over time by a counter represent a numerical value.

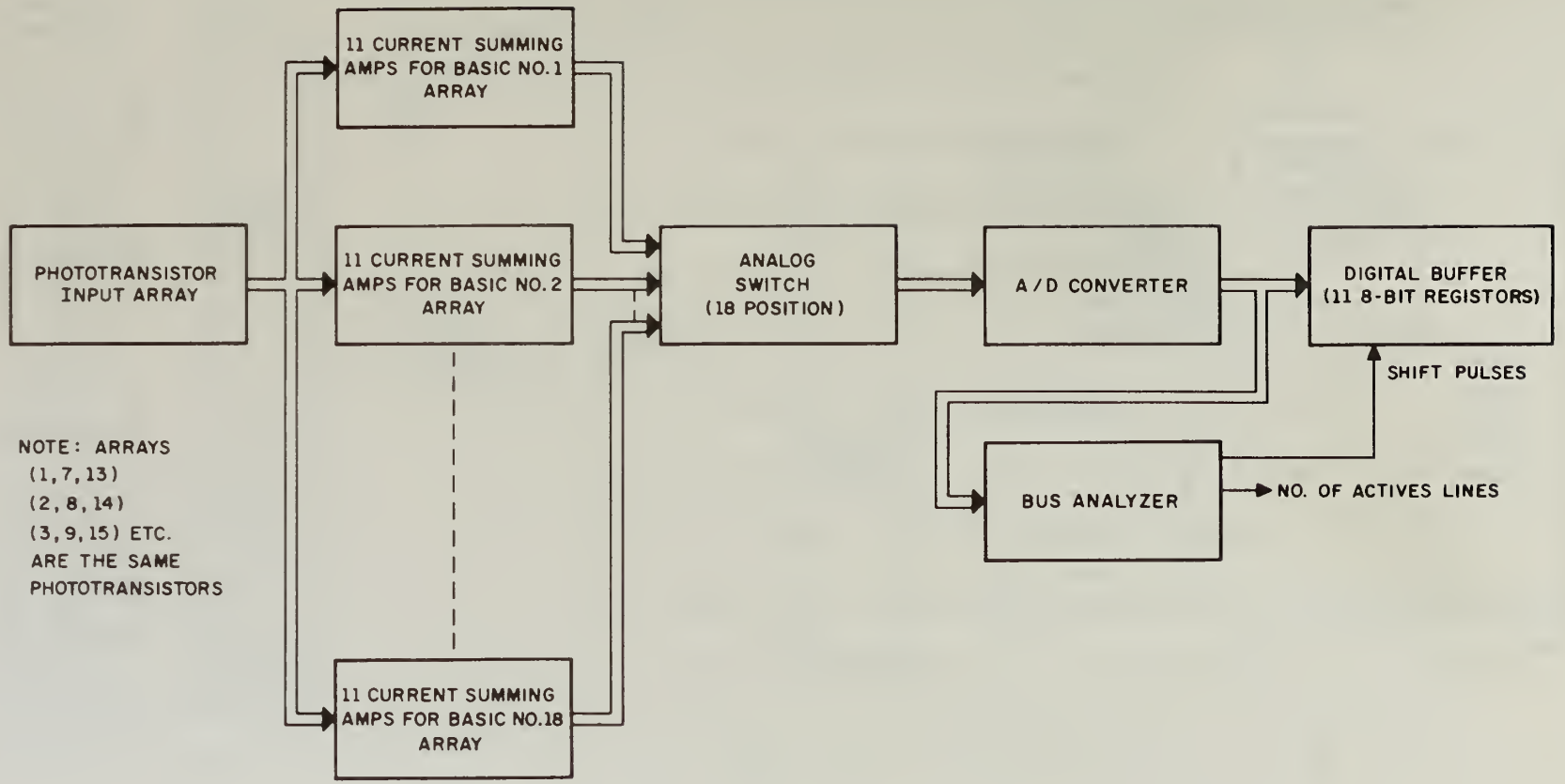


Figure 3.1 NORMAN Block Diagram

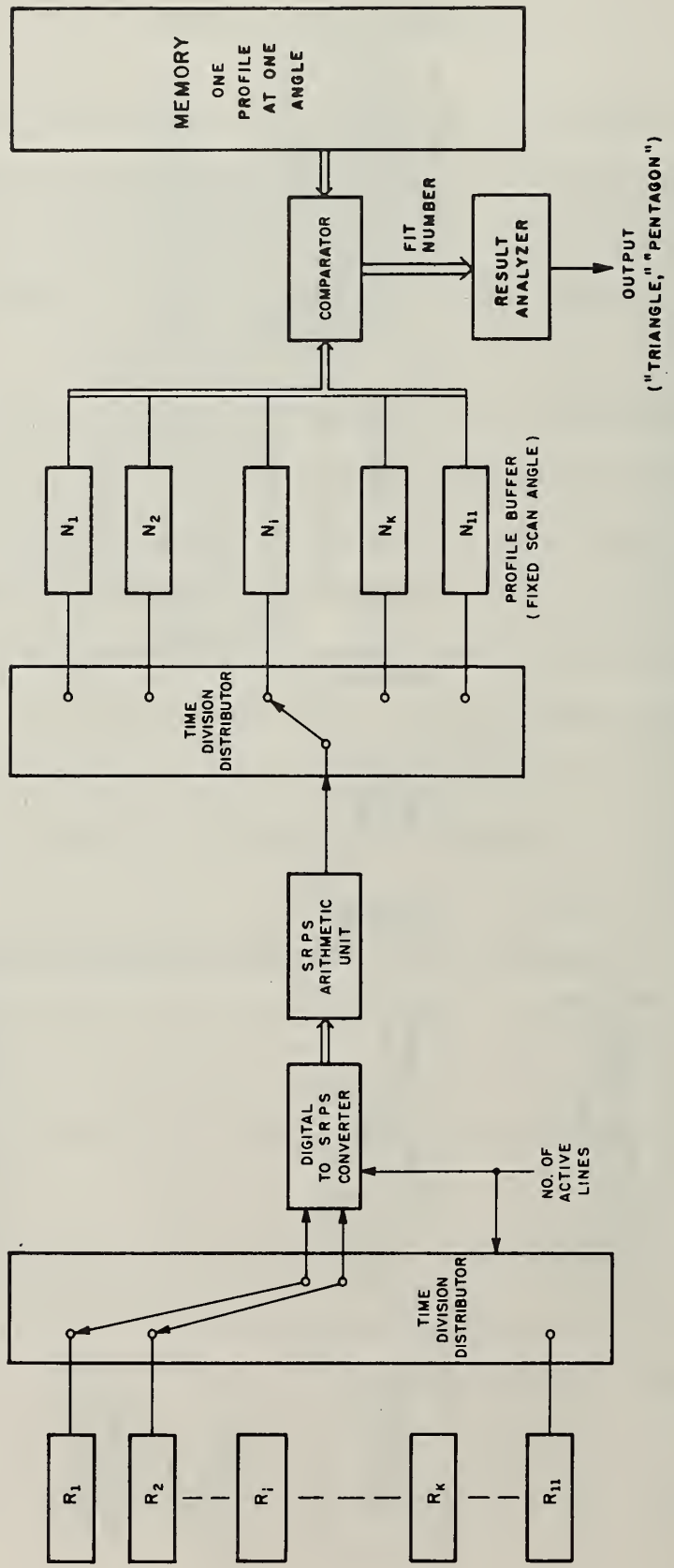


Figure 3.2 NORMAN Block Diagram

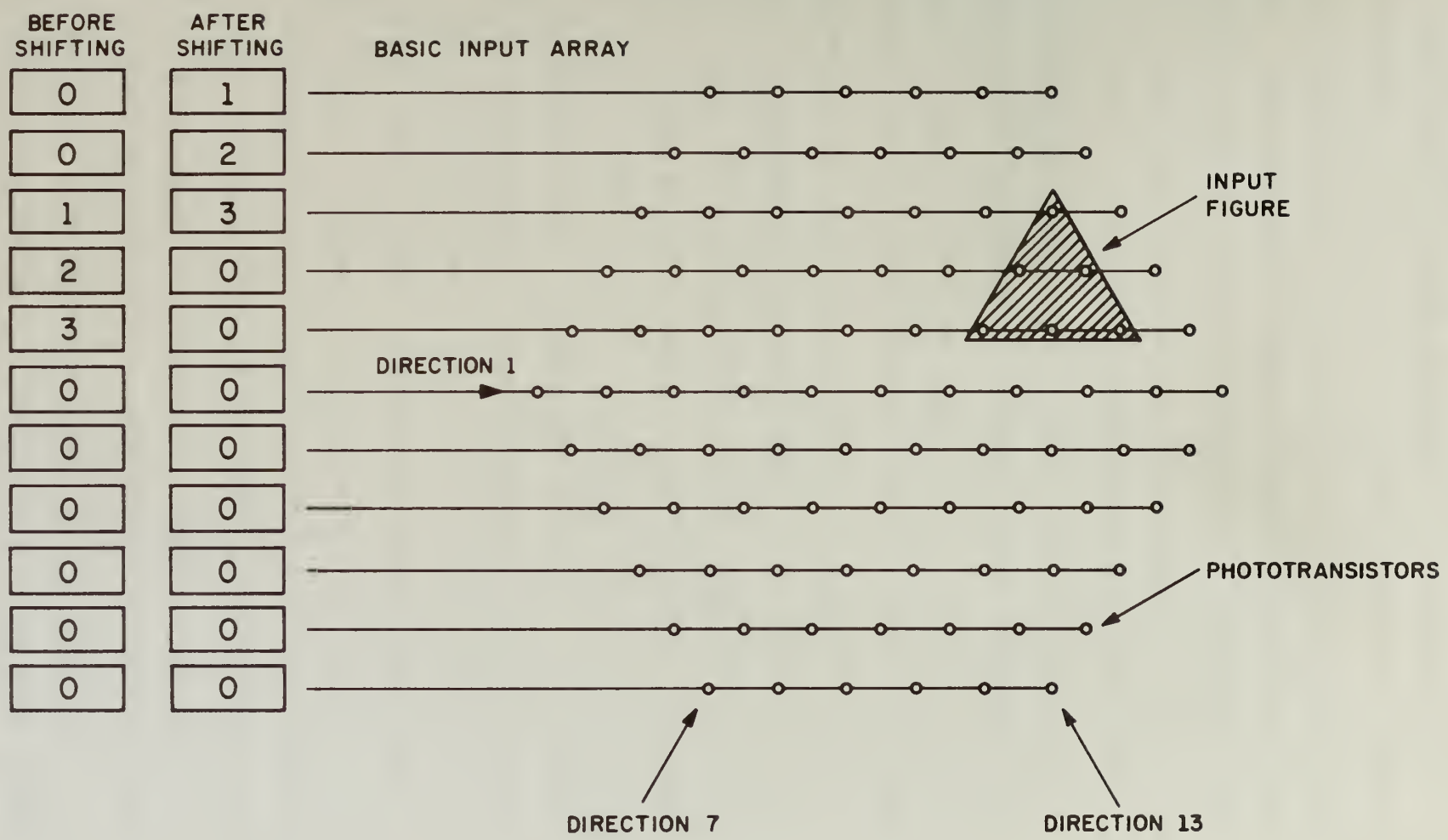


Figure 3.3 Bus Analyzer Shifting Action

Size independence is gained by sampling over the number of active lines during a certain fixed period of time. In other words, the number of active lines controls the switching rate of the first time division distributor: a larger figure requires a higher switching rate than a smaller figure, it having more lines to cover in exactly the same amount of time. Two registers are sampled at once because the SRPS arithmetic unit can be made to switch gradually from one to the other.

The output of the arithmetic unit is a single SRPS signal which varies almost linearly in time with respect to the profile of the input figure. The second time division distributor switches this signal during the same fixed period of time into eleven counters which serve as the profile buffer. At the end of the time period the profile buffer contains the profile of the input figure which is both position and size independent. A comparison is then made between each register of the profile buffer and a corresponding register of a profile buffer of a figure stored in memory. This comparison results in a number for each pair of registers which is equal to the absolute difference of the numbers in the registers. These absolute differences (eleven in all) are then summed together to give a number called a "fit" which is a direct measure of how closely the two profiles match. This comparison process occurs for each memory location of which there are five, making storage of five separate figures possible. A Result Analyzer Board then searches for the lowest difference or best fit and stores the name of the figure contained on the Memory Board with the best fit. This completes the process for one scan angle. To recognize the figure under conditions of rotation this process has to be gone through eighteen times (a 180 degree look at the figure with 10 degrees of resolution). Each time the Result Analyzer Board stores only the best fit and the name of the figure stored on

the Memory Board from which it came. At the end of its eighteen cycles, the result is displayed.

It should also be mentioned here that the profile buffer uses RAM type storage. This necessitates two modes of operation for the machine, STORE and ANALYZE. ANALYZE has been discussed above. STORE is similiar, the only difference being that instead of comparing between the two profile buffers, the numbers from the first profile buffer are dumped directly into the memory profile buffer. Also since only one angular view of a figure is stored in memory, the STORE operation is complete after one cycle instead of eighteen.

4.0 MACHINE DESCRIPTION

This section contains board by board description of the machine and should give a much clearer picture of how the processing is actually done. We start with a description of the front panel and how to operate the machine.

4.1 Front Panel

The front panel contains two rotary switches, a MODE switch and a NAME switch; two pushbutton switches, ERASE and ACTUATE; a double throw (normally centered) toggle switch labeled THRESHOLD, UP and DOWN; and two displays, one which displays the NAME and the other which displays the BEST FIT.

The first thing to do after turning NORMAN on is to set the threshold to some suitable value (see Section 4.8). This is done by turning the MODE switch to THRESHOLD SET and entering counts in the threshold counter by moving the threshold toggle switch to UP or DOWN. The threshold counter can also be reset by pushing ERASE.

There are five storage locations in NORMAN and each one must either be loaded with a figure or erased. To store a figure in memory location one set the MODE switch to STORE 1. Choose a figure to be stored, lay it on the phototransistor array, and select its name by means of the NAME switch. Pushing ACTUATE then starts the cycle and after it is complete, the name of the figure is displayed and the total number of counts in the profile buffer of that memory location is displayed by the BEST FIT display. In like manner all the storage locations can be filled simply by selecting the storage location with the MODE switch. Any location can also be erased by selecting it with the MODE switch and pushing ERASE.

To have NORMAN analyze what a figure represents, set the MODE switch to ANALYZE and push ACTUATE. After the processing is done (about 1/2 second) it will display the name of what it thinks the figure resting on the phototransistor array is. It will also display the best fit, which is a measure of how closely the figure laying on the phototransistor array and the figure it selected from memory match.

It should also be mentioned here that NORMAN has a library of eleven figures prepared for it. These were prepared photographically on large film sheets and appear as black opaque figures on transparent plastic sheets. The names of these figures also appear on the NAME switch. The library consists of: CIRCLE, TRIANGLE, RECTANGLE, PENTAGON, HEXAGON, CROSS, and the numbers 4, 5, 7, and 8.

4.2 Input Boards

The Input Boards were described quite fully in Chapter 2. Each one of the eighteen Input Boards provides one angular view of the figure to be recognized. Each contains eleven MC1741CP op amps and three CD4016AE four channel analog switches. Each op amp does current summing from a row of phototransistors in the array so that its output voltage is dependent upon the number of phototransistors on or off in that particular row. The four channel analog switches act as multiplexers to switch all eleven analog voltages onto a bus of eleven lines when a SWITCH SIGNAL is present at that board.

4.3 A/D Board

This board serves to digitize the eleven analog voltages present on the bus. It is driven by a twelve bit synchronous counter, the middle four bits of which are used to generate a staircase by the use of a high speed

op amp. The middle four bits are used because a new SWITCH SIGNAL comes to an Input Board at the same time that the counter starts and using the middle four bits ensures that the analog voltages are all stable before actual digitizing begins. By referring to Figures 4.1 and 2.3, we note that the amplifier configuration is nearly the same in each case. Each sums current through resistors which are switched on and off from a +12 volt line, in one case by the phototransistors and in this case by open collector high voltage buffers driven by counter bits five through eight. Each configuration also uses a biasing resistor down to a -12 volts. This close matching is very deliberate. If either or both supply voltages drift, both the analog voltages and the steps of the staircase drift in the same manner so that the correct digitized version on the analog voltage is still obtained.

The eleven analog voltages and the generated staircase go to eleven SN72510 comparators (Figure 4.2). The output of the comparator switches to a logical one when the staircase voltage steps above the analog voltage level. This change goes through a flip-flop to a NAND gate to shut off a train of pulses called STROBE pulses. The outputs of this board are the eleven STROBE lines and the bits of the counter. They all go to the next board, the Analysis Board, which works in conjunction with the A/D Board to digitize the analog voltages.

4.4 Analysis Board

The Analysis Board contains eleven four-bit shift registers which store the digitized profile (Figure 4.3). Counter bits five through eight of the A/D Board go to the parallel loading inputs of the eleven shift registers. Each of the eleven STROBE inputs goes to a shift register and keeps loading in the counts until the comparator on the A/D Board shuts it off. Since counter bits five through eight are also the ones that generate the staircase, each one of the

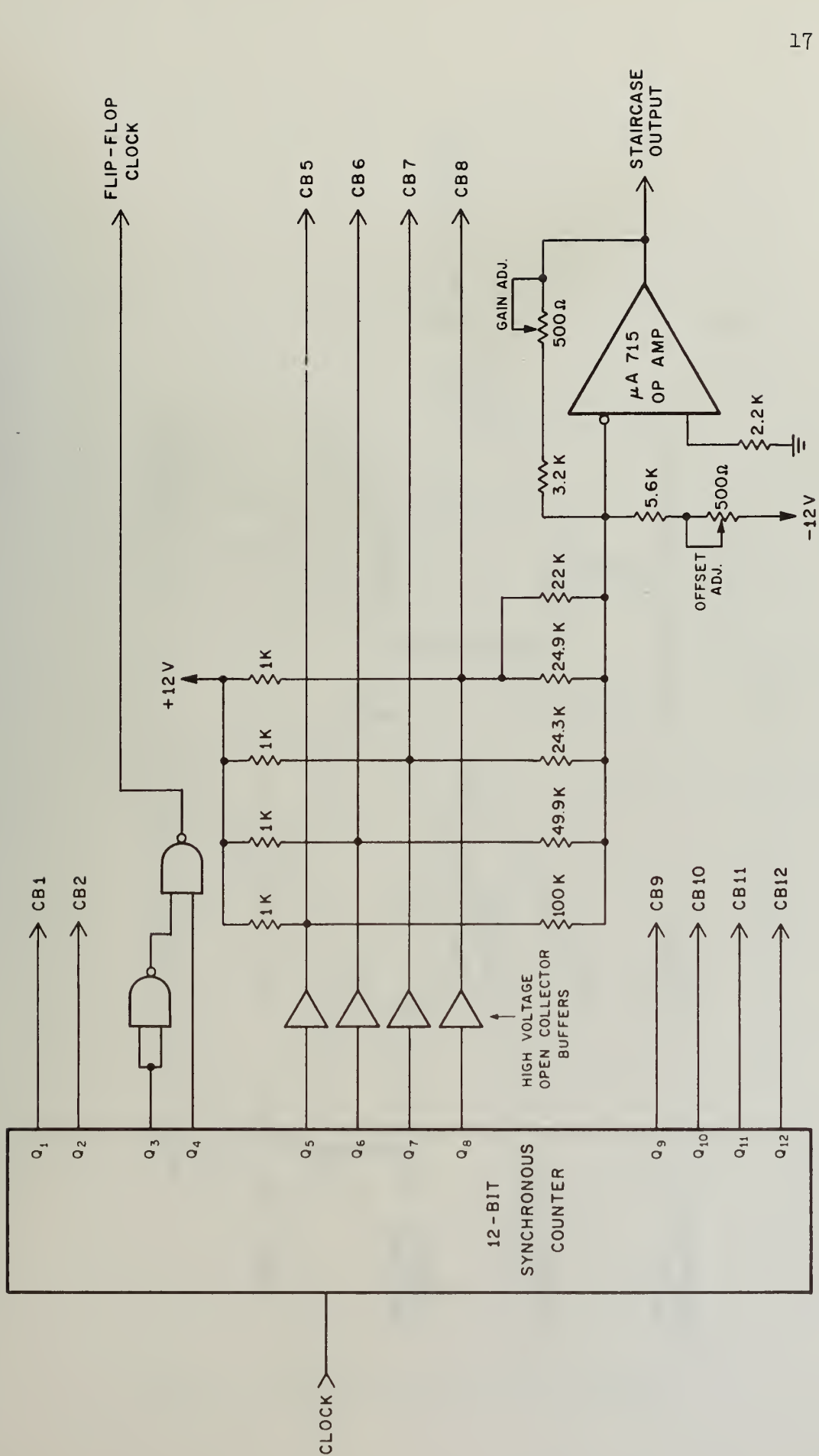
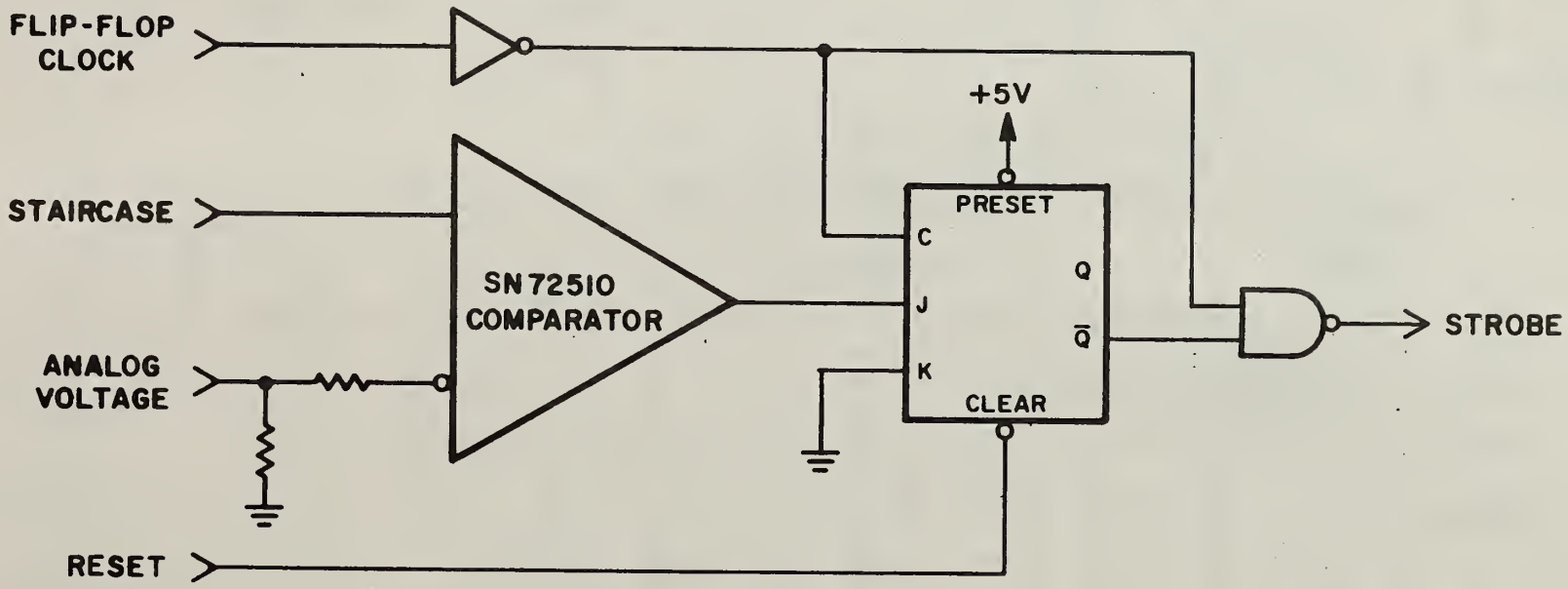


Figure 4.1 A/D Board Staircase Generator



NOTE: THE A/D BOARD CONTAINS 11 OF THESE CIRCUITS

Figure 4.2 Comparator Section of A/D Board

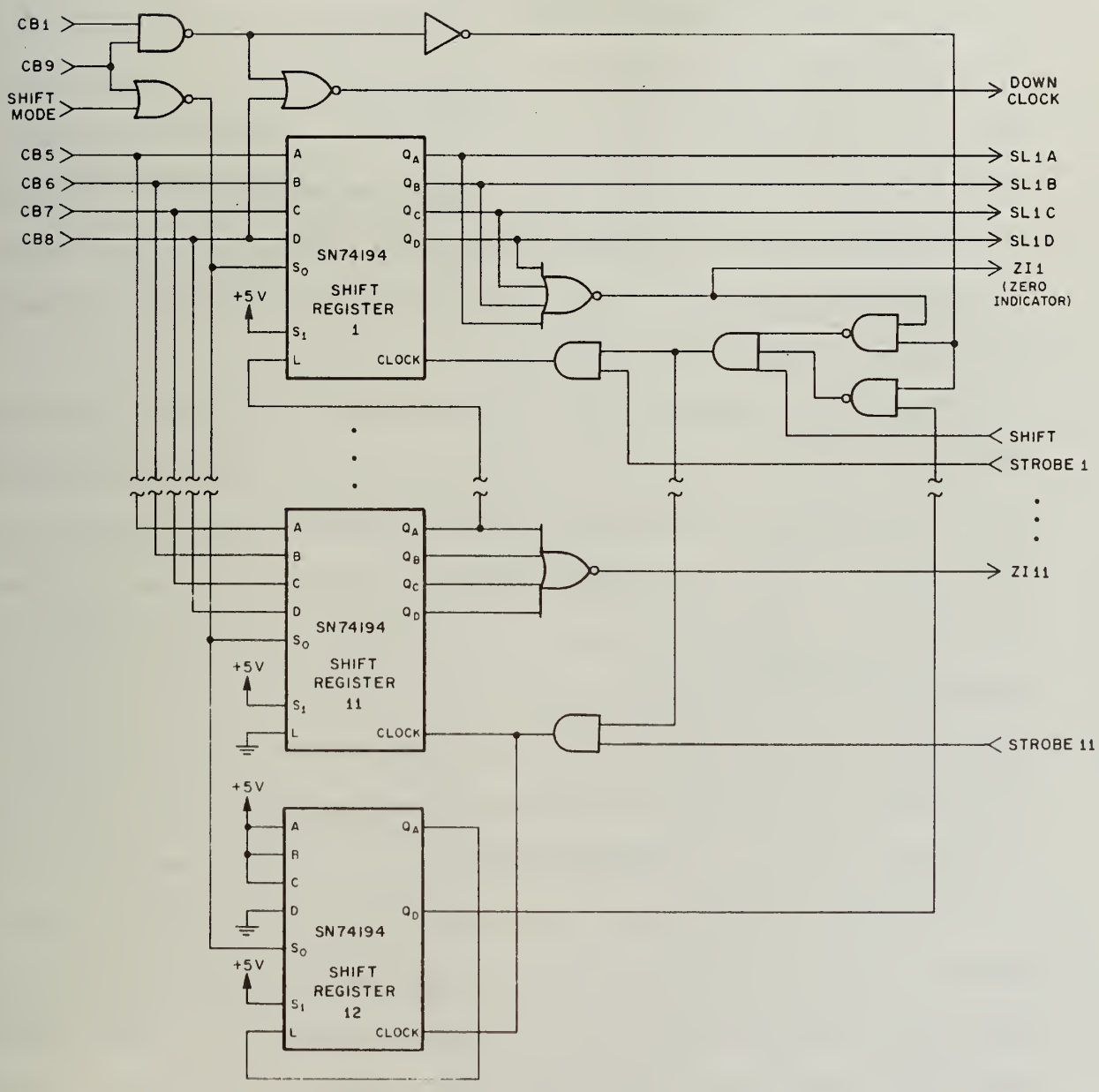


Figure 4.3 Buffer Section of Analysis Board

eleven shift registers contains the correct digitized version of its analog voltage after its strobe pulses have been cut off.

The Analysis Board has essentially two tasks to perform before its work is complete. It must shift all the four digit numbers up from one shift register to the next until the first shift register no longer contains the number zero: this gives the profile positional independence. The second operation is to discover the width of the profile. A down counter starts with shift register eleven and counts down from eleven until the first shift register containing a non-zero number is encountered (Figure 4.4). This technique was favored over a straightforward counting up scheme to prevent problems with profiles having "holes" in the middle.

Counter bit nine (CB 9) going to one informs the Analysis Board that the digitizing is complete and that it can start the two processes described above. Accordingly CB 9 switches the shift registers from the parallel loading state to the shift left state. Four input NOR gates are used to sense the number zero for each shift register. CB 1 provides the pulses to shift the numbers and a twelfth shift register is used to ensure that the shift pulses occur only in groups of four. If the NOR gate for the first shift register senses that the number zero is present, the NAND gate network lets through a shift pulse and the twelfth shift register ensures that three more follow it. After the four shift pulses, the number that was in the second shift register is now in the first and likewise with all the rest with the eleventh being loaded with all zeroes. This process continues until the first shift register no longer contains the number zero. After this shifting is complete, the up-down counter operating in the down mode and loaded with the number eleven samples the NOR gate of each shift register through a multiplexer and counts down until it finds the first shift register with a non-zero number.

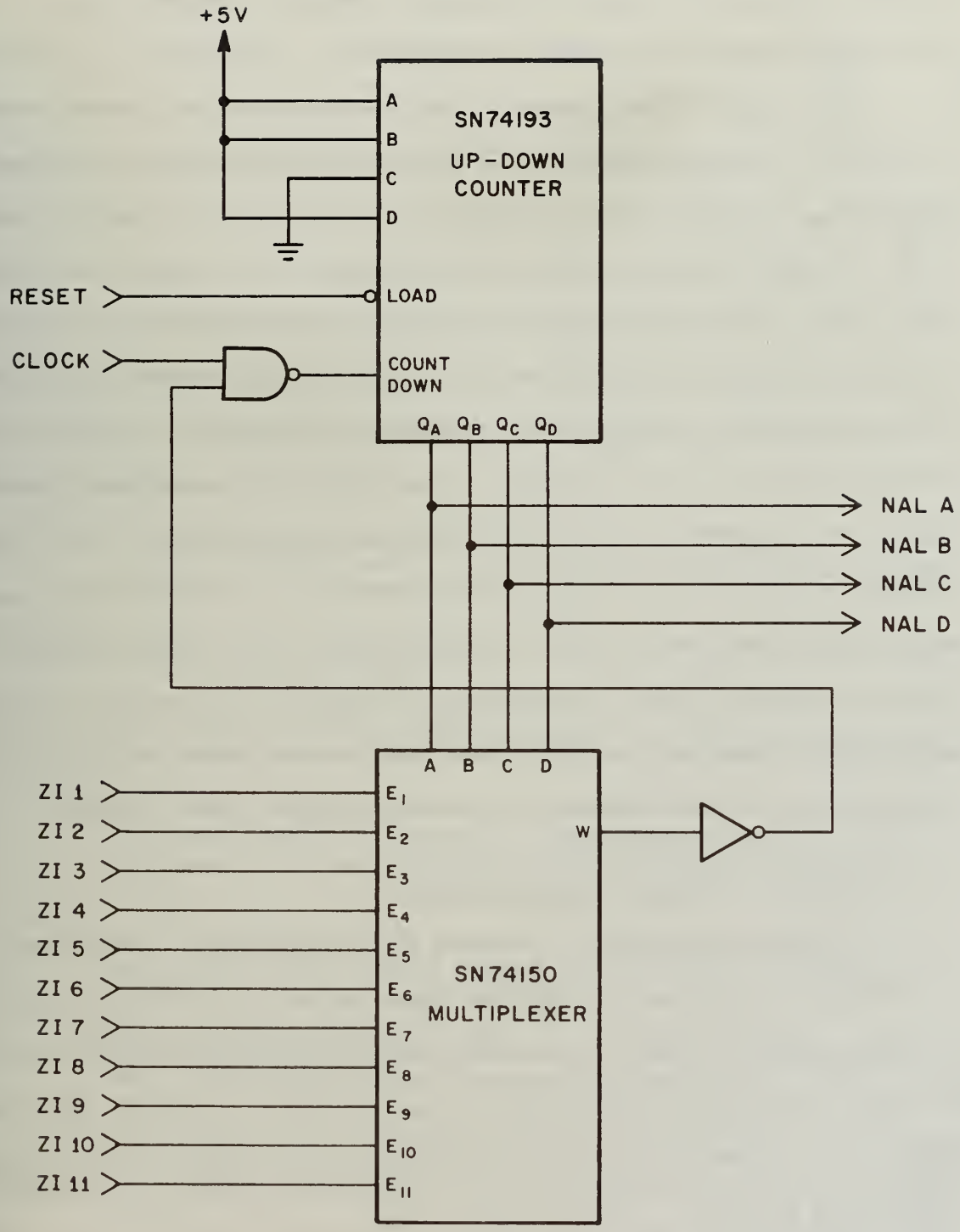


Figure 4.4 Number of Active Lines Information Section of Analysis Board

The number left in the counter after this process is complete informs the rest of the machine of the width of the profile.

There are two other inputs to the board not directly related to any of the above mentioned processes. These are the inputs labeled SHIFT and SHIFT MODE. Note that both the A/D Board and the Analysis Board are controlled by the counter on the A/D Board. When CB 11 goes to a logical one, the counter shuts itself off and the two boards sit there waiting for the next reset pulse to come along. Referring to the block diagram of Figure 3.2, the time division distributor samples only two registers at once for conversion to synchronous random pulse sequences. To actually do this sampling with multiplexers would require quite a bit of circuitry and board space. The scheme used instead is to only bring out the outputs of the first two shift registers and provide for external control of the shifting of the eleven registers. The SHIFT MODE input is used to put the shift registers into the shift left mode and the SHIFT input is a series of four small pulses coming from the Control Board which shifts the contents of one shift register into the next.

4.5 Stochastic Sequence Generator Board

This board generates all the main clock signals used by the rest of the machine and also converts all the necessary numbers into synchronous random pulse sequences (SRPS). The method used to generate the SRPS pulses is the (completely digital) recirculating shift register technique. This method is quite well documented and the bibliography lists several sources which discuss this method.

The particular shift register configuration in NORMAN has feedback from the 13th and 31st stages through an Exclusive-OR gate to the first stage. This shift register generates what is known as a maximal length sequence. That is, it goes through $2^{31}-1$ combinations of ones and zeroes before repeating itself. Only the sequence of all zeroes is avoided.

SN7485 four bit magnitude comparators are used to convert four bit numbers into SRPS pulses. A four bit number comes into the B inputs of the comparator and can be thought of as a threshold level. The A inputs to the comparator come from any four bits of the recirculating shift register and can be thought of as a digital noise input. The comparator emits a logical one when A is less than B or when the noise is below the threshold. From this one can see that the higher the particular number is, the greater is the probability of finding a one on its SRPS line which is the output of the comparator. NORMAN needs six different numbers converted into SRPS pulses. They are as follows:

(1) SL 1 (Scan Line 1) is the four bits of the first shift register on the Analysis Board. It is a partial representation of the profile of the figure.

(2) SL 2 (Scan Line 2) is the four bits of the second shift register on the Analysis Board.

(3) NAL (Number of Active Lines) is the four bits of the counter on the Analysis Board which tell the size or width of the profile.

(4) SF (Scale Factor) is used to scale the result on the Stochastic Arithmetic Board to prevent it from being too close to zero or one. It is a four bit number which is permanently wired to a value.

(5) GSV (Gradual Switching Value) is a three bit number coming from the Control Board and is used by the Stochastic Arithmetic Board to gradually switch from SL 1 to SL 2.

(6) $\overline{\text{GSV}}$ ($\overline{\text{Gradual Switching Value}}$) is the bit-wise complement of GSV and is also used by the Stochastic Arithmetic Board for switching.

The total number of bits sampled from the recirculating shift register is twenty-two. These are taken from the first twenty-two bits of the shift register and to ensure that all the numbers are mathematically independent, the shift register has to be shifted twenty-two times before another comparison can be made. In NORMAN, comparisons occur continuously, but each of the six SRPS lines are sampled only once every twenty-two time periods and stored in a shift register.

4.6 Stochastic Arithmetic Board

The Stochastic Arithmetic Board takes the six SRPS lines generated by the previous board and carries out the equation:

$$\frac{((SL\ 1 \cdot \overline{GSV}) + (SL\ 2 \cdot GSV)) \cdot SF}{NAL} \qquad (4.1)$$

Figure 4.5 shows a block diagram of the circuitry required to implement this equation. The SRPS arithmetic blocks required are a multiplier, an adder and a divider. Each of these are described below with the hope of giving an understanding of this type of processing without being mathematically rigorous. For those interested in stochastic processing itself, the thesis by Afuso listed in the bibliography is especially recommended.

4.6.1 Multiplication

Each SRPS line is assigned a numerical value according to the probability of finding a logical one on it during any time slot. Consider an example of two SRPS lines each having a value of 1/2. Then the probability of finding a one on either line in any time slot is 1/2. Stated another way, over a long period of many time slots, 1/2 of them will contain ones for each line. If the pulses on each line are random (synchronous with the time slots but randomly placed) and the two lines are independent of each other, the probability of a pulse occurring on each line in the same time slot is 1/4. This is of course the correct numerical result of multiplying 1/2 by 1/2. Detecting coincidence requires only an AND gate making the SRPS system probably the best number representation system ever devised to carry out multiplication.

4.6.2 Addition

Addition is as easy to realize intuitively as multiplication. Take an example of two SRPS lines each having a value of 1/4. The result of adding

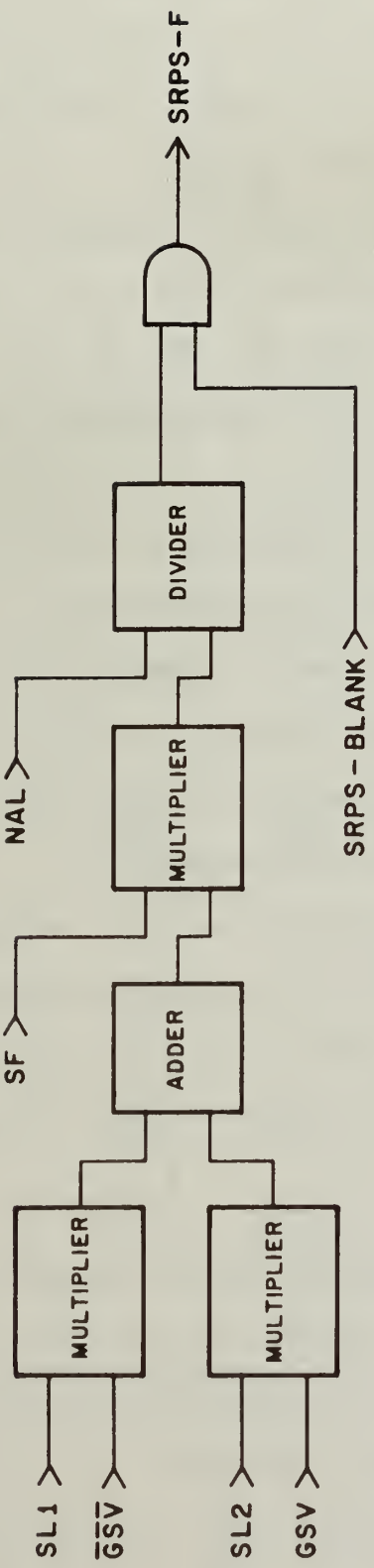


Figure 4.5 SRPS Arithmetic Board Block Diagram

these two lines should be 1/2. If each input has 1/4 of its time slots filled and the result should have 1/2 of its time slots filled, it is easy to see that each pulse on each input line should result in an output pulse. The idea which immediately comes to mind is to use an OR gate. This works fine as long as pulses do not occur on each input simultaneously: if two pulses do come in, the OR gate only outputs one. This extra pulse has to be stored, so that it can be inserted into the output later when there is a free time-slot in which neither input line has a pulse present.

The easiest way to implement this is to use an up-down counter to store the coincident pulses. Every time a coincidence occurs, the counter is counted up by one. By means of a clock signal, a pulse is inserted into the output line every time there is a free time slot and the counter contents are not zero. This also decrements the counter by one. Circuitry must be added to prevent overflowing the counter or counting down past zero. Figure 4.6 shows the schematic of the adder.

The accuracy of this system depends on the capacity of the counter. In NORMAN a readily available four bit up-down counter is completely sufficient because the two input lines have the property that when one has a large value the other has a very small value and vice-versa.

4.6.3 Division

Division is the hardest operation to implement and the hardest to understand. The numerical value associated with an SRPS signal can be expressed as $u = f/f_o$, the average frequency of the signal pulses divided by the frequency of the time slots (the clock). For division, an SRPS must be generated such that its value $u_3 = u_1/u_2$. As Afuso states in his thesis:

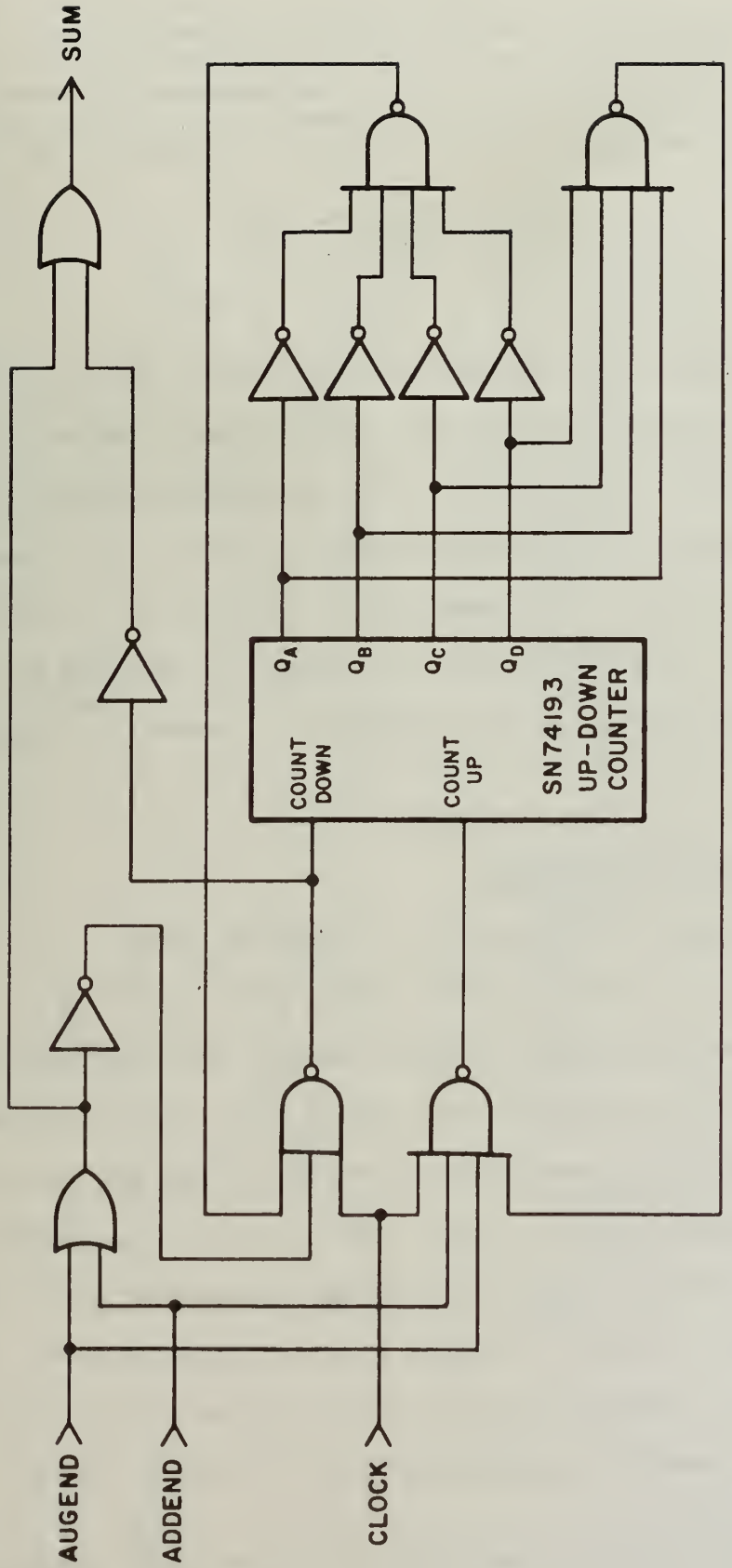


Figure 4.6 Schematic Diagram of an Adder

"Since $u_2 = f_2/f_o$, the average period of the divisor sequence expressed in terms of the clock period is given by $1/u_2$. If the number of pulses, given by the average period of the divisor sequence divided by the clock period, i.e., $1/u_2$, are generated for every pulse of the dividend sequence, the sequence generated in this way has as its average repetition rate $f_3 = f_1(1/u_2)$. In terms of the machine variable:

$$u_3 = \frac{f_3}{f_0} = \frac{f_1}{f_o} \cdot \frac{1}{u_2} = \frac{u_1}{u_2}$$

Thus the sequence gives the quotient u_1/u_2."[1]

The division algorithm then is to generate a series of pulses for every pulse of the dividend sequence. This series of pulses should start at the next divisor pulse and last until the following divisor pulse, thereby being as long as the instantaneous period of the divisor sequence following the dividend pulse. A storage unit is again needed to store dividend pulses that occur before the period of the divisor sequence is up. Figure 4.7 shows example sequences and Figure 4.8 is a schematic diagram of the divider.

4.6.4 The Equation Implemented

The numerator of Equation 4.1 contains the terms:

$$(\text{SL } 1 \cdot \overline{\text{GSV}}) + (\text{SL } 2 \cdot \text{GSV})$$

This part of the equation describes the gradual switching action from one shift register of the profile buffer to the next. GSV is generated by a counter on the Control Board which starts at zero and counts up to seven, then resets itself and starts again. $\overline{\text{GSV}}$ is the bit-wise inverse of GSV. Thus while GSV increases stepwise linearly from an SRPS value of zero (counter contents of zero) to an SRPS value of one (counter = 7), $\overline{\text{GSV}}$ decreases stepwise linearly from an SRPS value of one to zero. Since the two multiplication terms are summed together, it is evident that the sum at

---

[1] C. Afuso, "Analog Computation with Random-Pulse Sequences," University of Illinois, February 1968, pp. 77 and 78.

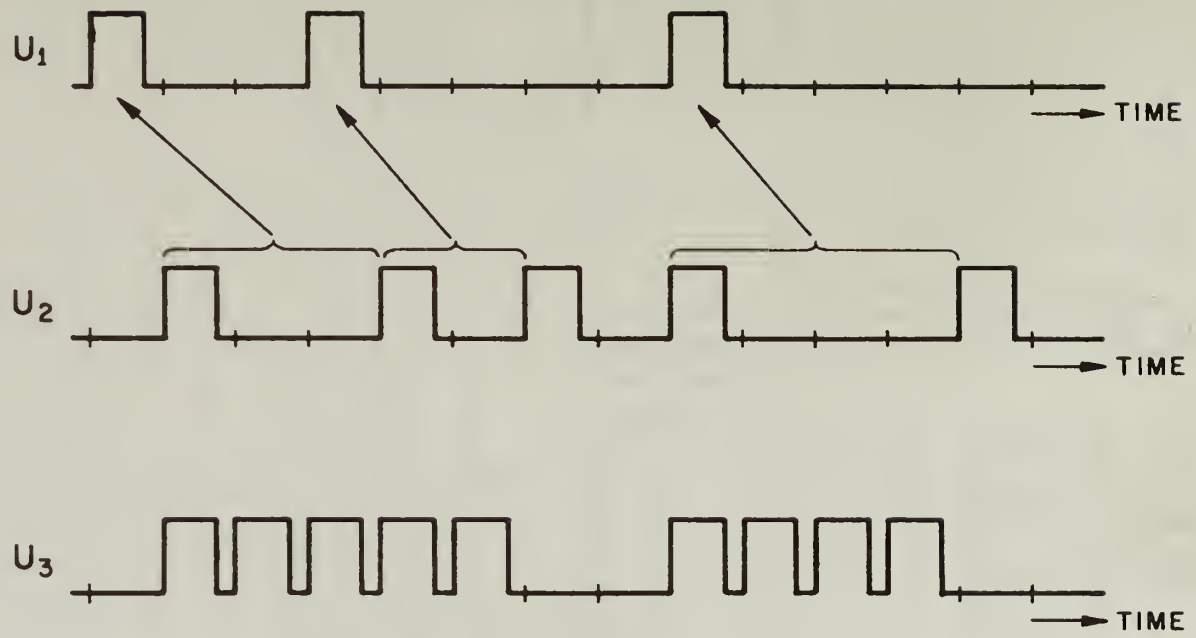


Figure 4.7 Dividend, Divisor, and Quotient Sequences Showing the Principle of Division

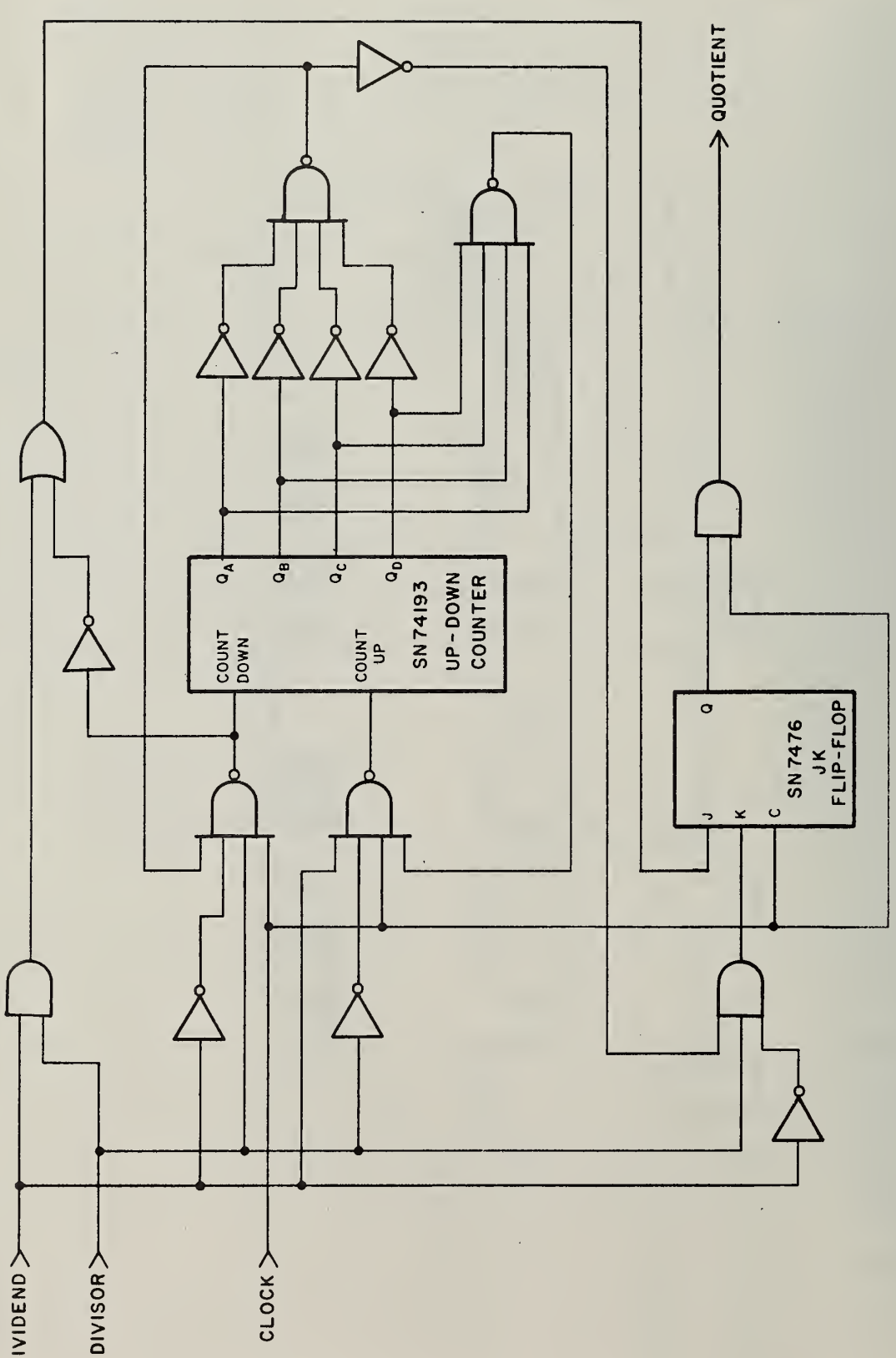


Figure 4.8 Schematic Diagram of Divider

first depends entirely on SL 1 because $\overline{GSV}$ = 1 and GSV = 0. This slowly changes as the counter counts up until $\overline{GSV}$ = 0 and GSV = 1 and the sum then depends entirely on SL 2. In this manner gradual switching from one register to the next is accomplished.

When the counter on the Control Board resets itself, it also sends out shift pulses to the Analysis Board which shifts the contents of SL 2 into SL 1 and SL 3 into SL 2, etc. Therefore immediately before the reset occurred, the sum depended entirely on SL 2 and immediately after it occurs, it also depends entirely on SL 2. This dependence then decreases and SL 3 takes over. In this manner the profile is smoothly expanded in time. The amount of expansion depends on the width of the profile because every profile is expanded to a uniform size of eleven buffers wide.

The above mentioned expansion is in one dimension only, i.e., the width of the figure. Since the figure is two-dimensional, it must be expanded in the other direction as well, to preserve the correct profile. The amount of expansion necessary is inversely proportional to NAL, the width of the figure. Therefore the SRPS sum is divided by NAL in the manner of Equation 4.1 to completely normalize the profile with respect to size. SF in the equation is a constant used for scaling the result.

An inspection of the block diagram of Figure 4.5 also shows an AND gate at the output SRPS. This enables the Control Board to completely shut off the SRPS signal. It has a very important use which will be discussed in Section 4.12.2.

4.7 Memory Boards

There are five memory storage locations in NORMAN, each one requiring two boards because of the extensive amount of processing required at each location. The two memory boards are called "Memory Board A" and "Memory Board B" and the logic is split up according to function.

Memory Board A (Figure 4.9) has three four-bit SN74193 up-down counters to count the SRPS-F pulses (the output of the SRPS Arithmetic Board) and a flip-flop to control the direction of counting. It also has three SN7489 random access memories to store the normalized profile. This profile storage has been and will be described as a profile buffer with eleven registers but in reality it is this RAM type storage with each register being a particular address of the RAM.

Memory Board B (Figure 4.10) has four four-bit SN7483 adders and five SN74194 shift registers, four of which store the output of the adders and one which stores the name information. This board also contains twenty open collector NAND gates whose outputs go to a twenty line RESULT BUS and permit each of the memory boards to put its results on the bus on command.

Keeping in mind that the circuitry is split up, the operations of the boards will be described as a whole with no further mention of what is actually on which board.

The activity of the memory boards is divided up into eleven time periods, one for each memory location of the profile buffer. At the border line of any two time periods, a sequence of three events happens. First, a short pulse called MCP 1 (Memory Clock Pulse 1) comes along, then the address is incremented by one, and finally another pulse called MCP 2 comes along.

The memory boards have two modes of operation, "store" and "analyze." The two memory clock pulses are broken up into four distinct pulses, two of which are active during each mode of operation.

4.7.1 Store Mode

At the start of a machine cycle in the store mode, the memory boards receive a reset pulse which clears the counter and shift registers. Then beginning the first of the eleven time slots, an MCP 2 comes along which in

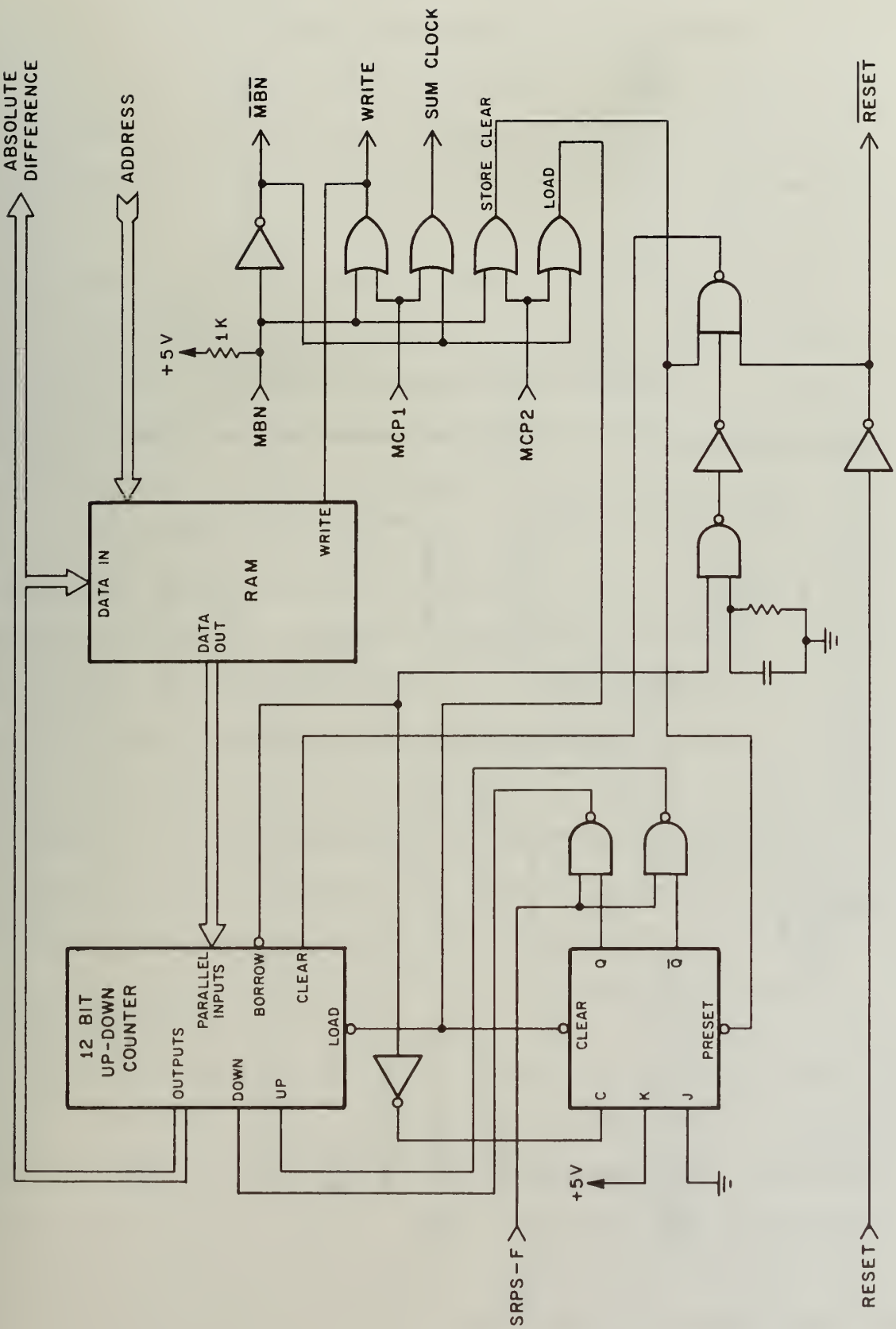


Figure 4.9 Schematic Diagram of Memory Board A

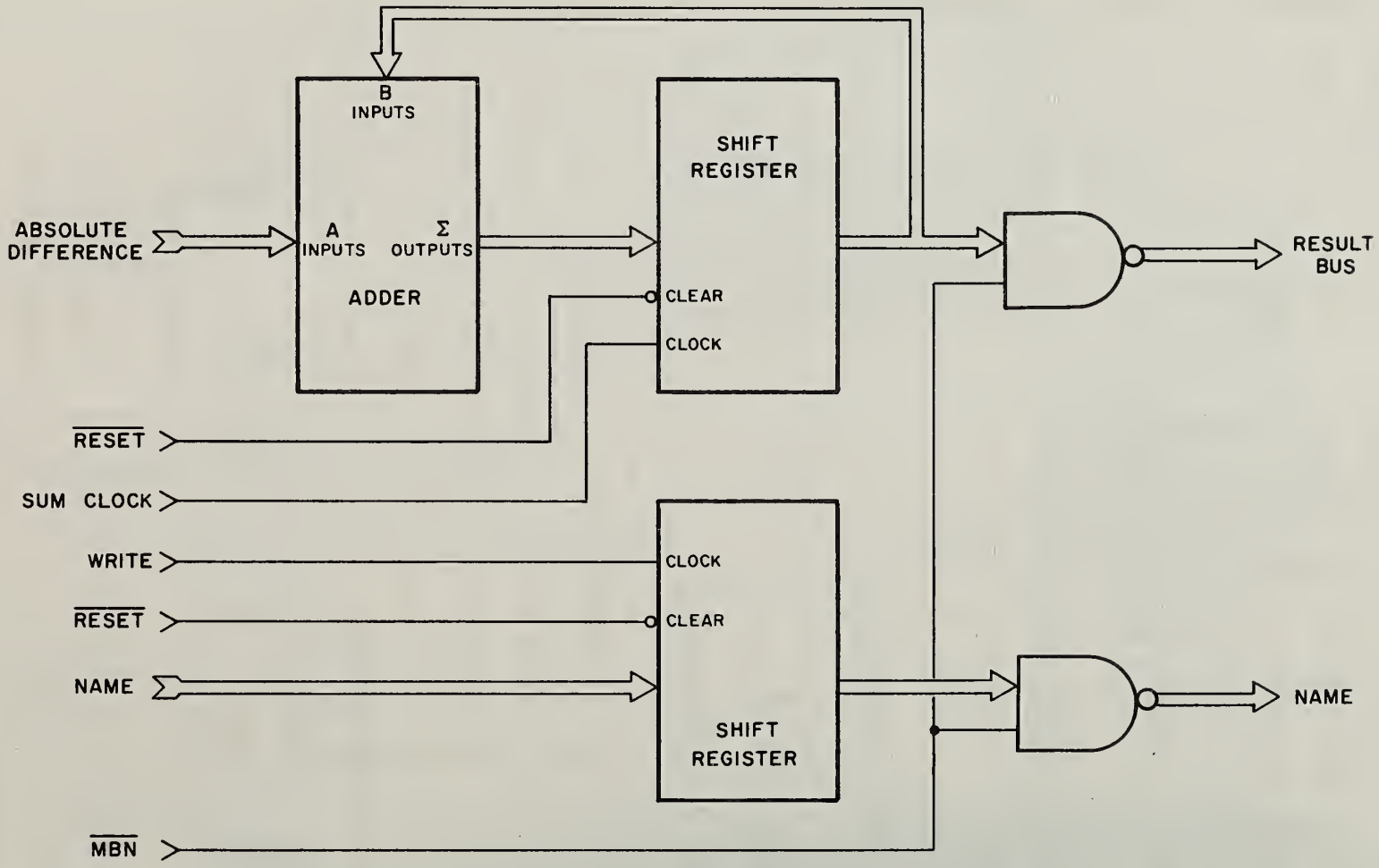


Figure 4.10 Schematic Diagram of Memory Board B

the store mode generates a STORE CLEAR which, in turn, clears the counter again and clears the flip-flop controlling the counting mode, putting it in the up mode. Then the SRPS-F pulses start coming in and are counted by the counter. At the end of this time slot the SRPS-F pulses are shut off and an MCP-1 pulse is received which in the store mode translates into a WRITE pulse. This strobes the contents of the counter into memory address location zero and stores the name information into a shift register.

At the start of time slot two the address location is incremented and an MCP 2 is again received and generates a STORE CLEAR. The SRPS-F pulses then start coming in again and are counted. This process continues over and over for eleven time slots and results in a filled profile buffer.

The memory boards are put into the store mode when the MBN (Memory Board Number) input is pulled low. Only one set of memory boards can be in the store mode at once and these are selected by the STORE switch on the front panel.

The memory boards also have an erase feature which can be activated in the store mode. When one of the five memory locations is selected by the STORE switch and an ERASE button is pushed, the name register at that particular location is cleared. This indicates to the rest of the machine that the results of that board are to be ignored.

4.7.2 Analyze Mode

At the start of a cycle in the analyze mode the memory boards receive a reset pulse which clears the counter and the shift registers. Beginning the first time slot, an MCP 2 is received which generates a LOAD pulse in the analyze mode. This LOAD pulse presets the counter to the number stored in address location zero of the profile buffer. It also presets the count mode control flip-flop into the down mode. Then SRPS-F pulses start coming

in and the counter keeps counting down until one of two things happens. The first is that the end of the time period occurs and an MCP 1 comes along. The second is that the counter counts all the way down to zero. When this happens, the count mode control flip-flop gets reset by the borrow output of the counter into the up mode and on the next SRPS-F pulse the counter starts counting up. It continues counting up until the end of the time period. At the end of the time period then the counter contains a number which is always equal to the absolute difference between the number of counts in the profile buffer and the number of counts received in that time period. This number gives a direct indication of how closely those two segments of the normalized profile agree or, the lower the number, the better the fit.

At the end of the time period, the SRPS-F pulses end and an MCP 1 comes along. In the analyze mode this generates a pulse called SUM CLOCK which goes to the shift register. The outputs of the counter go to the A inputs of the adder. The outputs of the adder go to the inputs of the shift register and the outputs of the shift register, besides going through NAND gates to the RESULT BUS, go to the B inputs of the adder. The result of this configuration is that the adder is continually adding the number stored in the shift register and the number in the counter. The SUM CLOCK pulse latches this new sum into the shift register.

To start the second time period, the memory address is incremented by one, an MCP 2 is received and the SRPS-F pulses start counting the counter down again. At the end of all eleven time periods, the shift register contains the sum of all eleven absolute differences. This sum tells how closely the two profiles fit each other.

4.8 Threshold Board

NORMAN has five storage locations which each can store the normalized profile of one figure. It has a prepared library of eleven figures. This clearly gives rise to the possibility that the machine could be asked to recognize something which has not been stored. The Threshold Board gives NORMAN the ability to take care of this situation.

The Threshold Board consists of an MBN input identical to that of the memory boards and an up-down counter made up of four SN74193 up-down counters (Figure 4.11). When storage location zero is selected by the STORE switch on the front panel, MBN is lowered and up or down pulses can be applied to the counter by the THRESHOLD switch on the front panel. The counter can therefore be set to any number and by means of sixteen open collector NAND gates, this number can be applied to the RESULT BUS. This counter then looks exactly the same to the rest of the machine as the shift registers of each memory location which store the fit numbers. If the threshold is properly set, when the machine is asked to recognize a figure which it does not have in storage, all the fit numbers will be greater than the threshold and the machine will display THRESHOLD as the result.

The Threshold Board also contains the switch debounce circuitry for the two pushbutton switches mounted on the front panel.

4.9 Result Analyzer Board

The Result Analyzer (Figure 4.12) is a very important board becuase it has to search the Threshold Board and the five memory locations for the best fit and send this result on to the Display Board for display. It accomplishes this task by means of a comparator made up of four SN7485 comparator chips and shift register storage of twenty bits, sixteen of which are used to store the name information. The B inputs of the comparator come directly

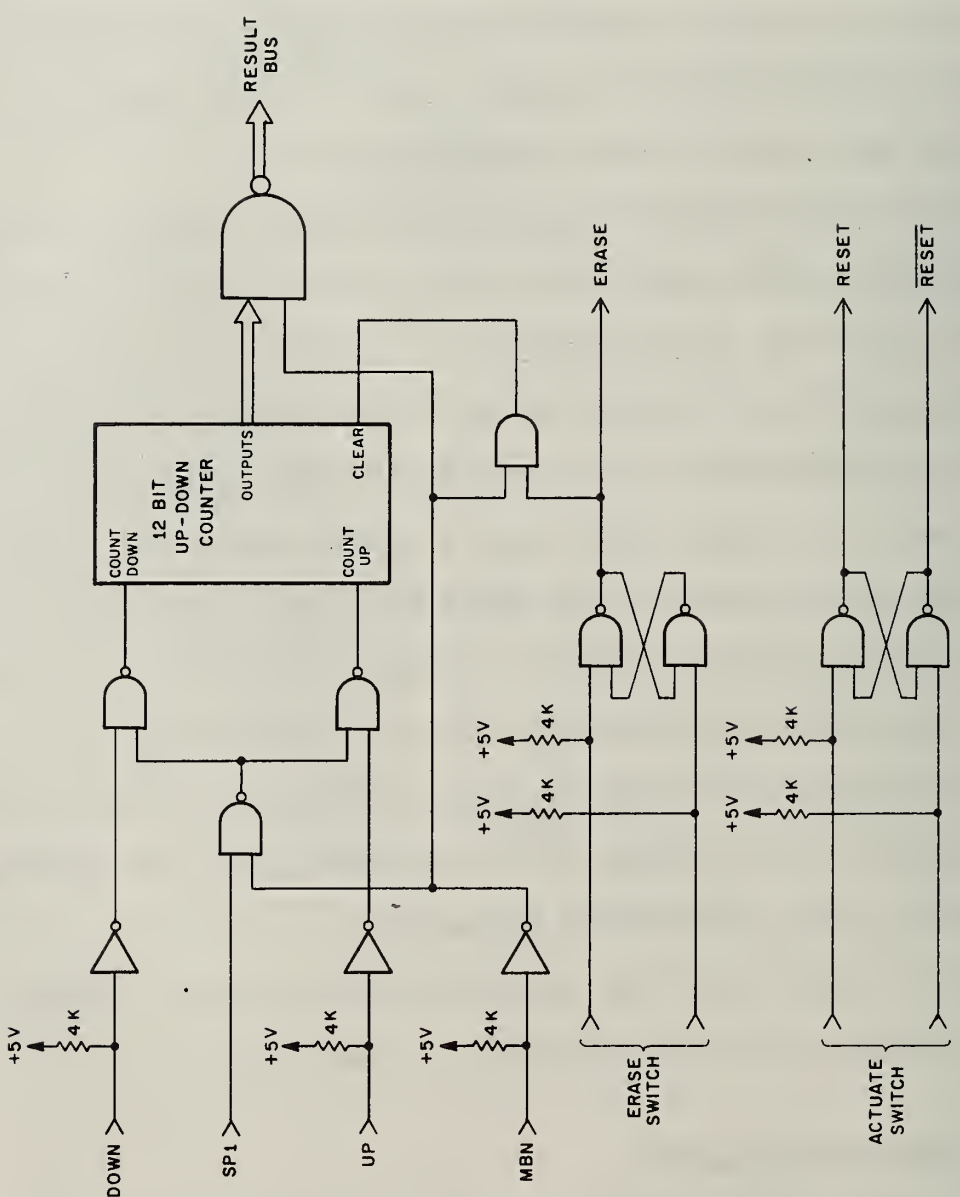


Figure 4.11 Threshold Board Schematic

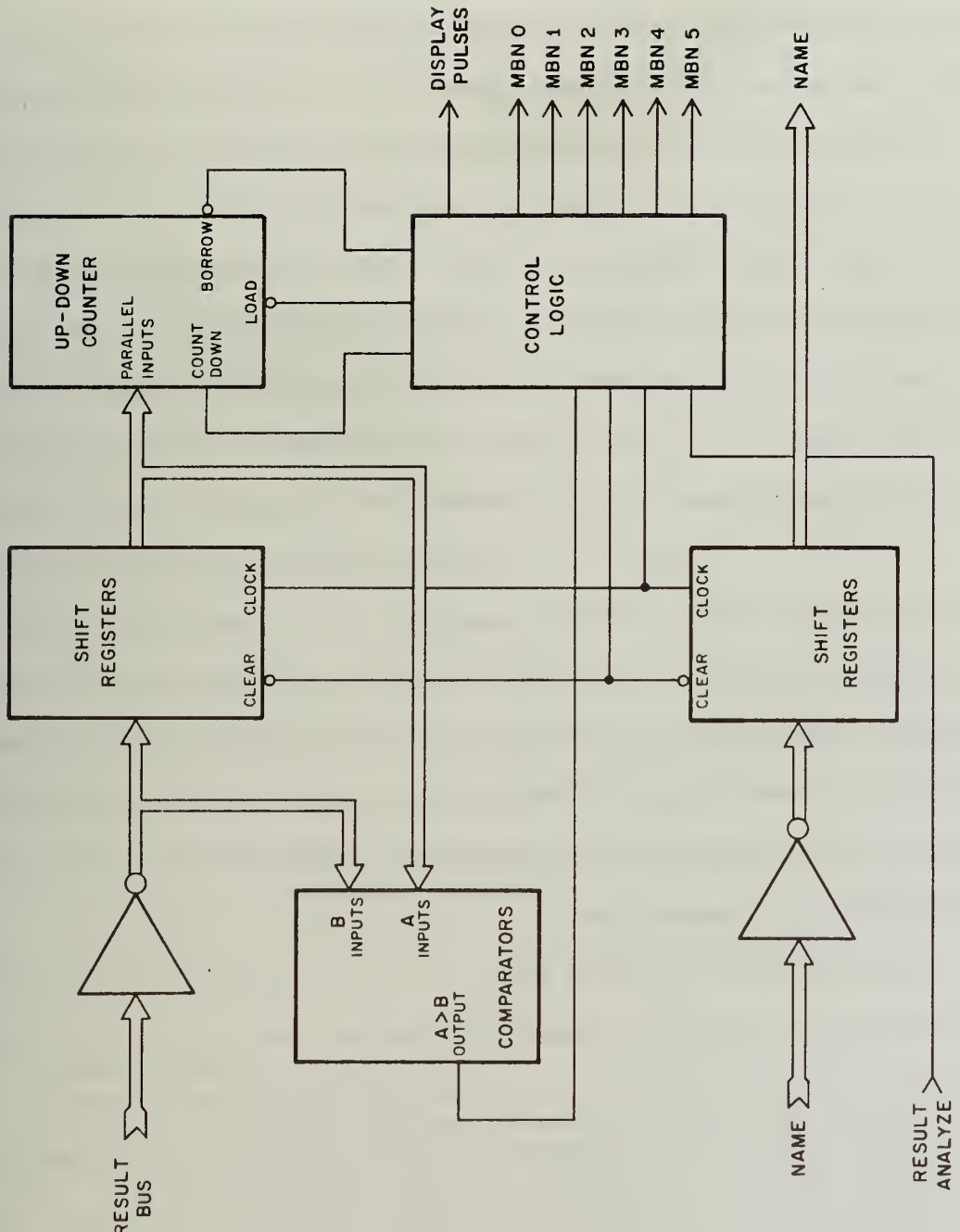


Figure 4.12 Result Analyzer Board Schematic

off the RESULT BUS while the A inputs come from the outputs of the sixteen shift register bits. The inputs to the shift register also come directly off the RESULT BUS. The output of the comparator indicates which number is smallest, the number in the shift register or the number of the RESULT BUS.

The Result Analyzer obviously cannot go to work until the memory boards are finished and have their fit numbers ready. This is indicated by a signal called RESULT ANALYZE going low. When the machine is in the analyze mode, this signal enables a counter which, through a demultiplexer, lowers each MBN signal in turn and thus puts the fit number of each memory location on the RESULT BUS. The sequence starts off with MBN 0, which is the Threshold Board, being lowered. Its fit number is then clocked into the shift register and MBN 1 is lowered. The fit number and name of memory location one are then clocked into the shift register only if its fit number is lower than the number currently in the shift register and if the name is not zero. (A zero name number indicates an erased condition for that memory location). It does this process through MBN 5 and at that time the shift register contains the lowest fit number and the name associated with it. This completes the process for one angular view.

The board remains inactive until the Control Board starts it again in its search for the lowest fit number from the next angular view. The only difference in the processing for the second and later views is that the shift register is not first loaded with the fit number from the Threshold Board since to do so would nullify all previous results. After this process has been gone through for all eighteen views and only the best fit and its name remain after all those comparisons, the result has to be displayed. In NORMAN, the Result Analyzer Board is in the lowest card nest in the cabinet, while the display is located in the very top of the cabinet. Since the number of wires connecting these two areas was great enough already, a scheme was

found to avoid running sixteen separate wires for the fit number digits. A multiplexing-demultiplexing scheme could have been used or, if there is plenty of time to transmit the information and particularly if the number has to be converted from a binary to a BCD format, the following technique is helpful. A down counter can be loaded with the fit number. Clock pulses are then applied to it and a wire going up to the Display Board. These pulses keep being applied to the down counter until it hits zero at which time they are also shut off to the Display Board. If a decimal counter on the Display Board has started counting up from zero on these pulses, it will now contain the correct fit number in BCD format.

The Result Analyzer Board does transmit the name information up to the Display Board by four wires.

The Result Analyzer Board is also used to display information when NORMAN is in the store mode. In this mode the counter and demultiplexer driving the MBN lines are disabled because the STORE switch is already pulling down an MBN line. In this mode information is clocked directly into the twenty bits of shift register storage and fed to the Display Board through the use of the down counter as before. No comparisons need be done in this mode.

4.10 Display Board

This board is used to display both the numerical fit information and the name information from the Result Analyzer Board. The fit information is displayed using five digits of seven segment readouts. The DISPLAY PULSES clock five digits of BCD counters whose information is then latched into five shift registers. Each shift register drives a BCD to seven segment decoder which in turn directly drives the display. See Figure 4.13.

The Display Board is also used to display name information which it receives as a four bit binary number. The four NAME lines go to a

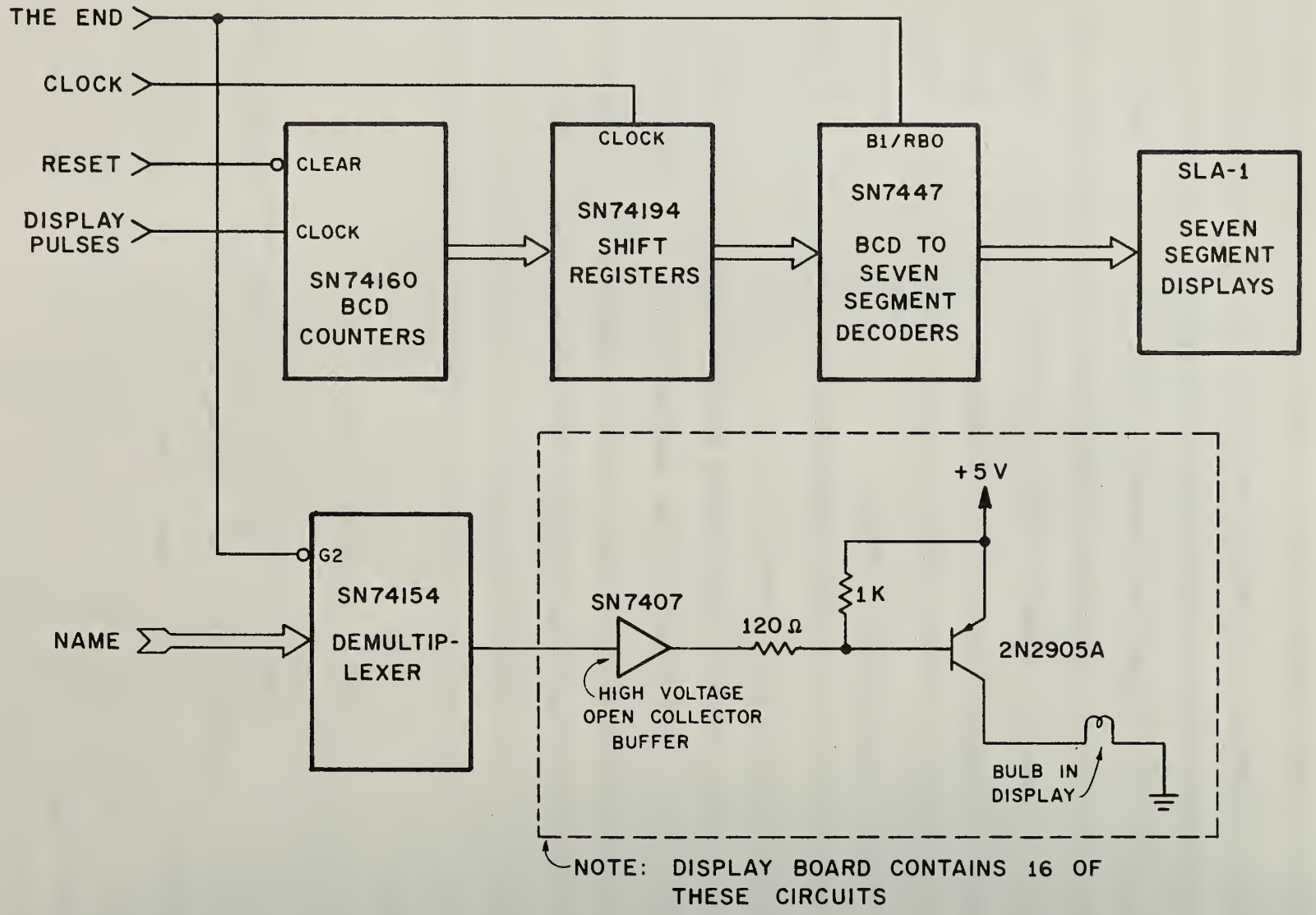


Figure 4.13 Display Board Schematic

demultiplexer whose sixteen outputs go to integrated circuit and discrete transistor drivers to drive incandescent bulbs in the display. The display is called a "One-plane Readout" and is manufactured by Industrial Electronic Engineers, Inc. It consists of an array of bulbs each of which illuminates a small area of a photographic negative directly in front of them. Through a series of lenses the information is displayed on a small frosted glass screen. Special negatives were constructed for NORMAN which contain the names of the figures making up the library. Therefore when the Display Board receives a particular name number you see displayed a name from the library like "TRIANGLE."

4.11 Switching Point Controller Board

Referring back to the description of the time division distributor in Chapter 3, we recall that it had to have a precisely controlled variable switching rate because in a certain set amount of time it had to switch over the number of active lines which could vary from one to eleven. This block of time then has to be divided up into eleven equal pieces, ten equal pieces, etc., all the way down to one piece. The most precise way to accomplish this is completely digitally. The Switching Point Controller Board contains a counter driven by a clock which drives the address lines of a read-only memory. The ROM has a connection only at an address where there is a switching point. All the switching points for a certain sequence are then OR'ed together so that the ROM has twelve outputs:

SP 0, a pulse at the start of the time period.
SP 1, a pulse at the end of the time period,
SP 2, a pulse in the middle and at the end of the time period,
SP 3, three equally spaced pulses in the time period, etc. to,
SP 11, eleven equally spaced pulses in the time period.

A short computer program was run to find a suitable number almost divisible by all the numbers from one to eleven to determine the size of

the ROM. This number was chosen to be 1440. The ROM then requires eleven address lines which makes it seem like quite a large memory but because it is so sparsely populated (few number of connections) it was still quite feasible to hard wire.

4.12 Control Board

The Control Board was the hardest to design and is the hardest to describe because it has the difficult job of controlling all the rest of the machine and getting it all to work together. The board can be broken down into four areas, each of which is described below.

4.12.1 Time Frame Generator

All the processing for one angular view of a figure happens during what is called a time frame. This section of the Control Board (Figure 4.14) uses a counter to generate the time frame. During count zero of the counter (right after ACTUATE has been pushed on the front panel) the A/D and Analyze Boards are active. By the time the counter is clocked to one, they have finished their tasks and the Analyze Board is holding the unnormalized profile ready for use.

At count one the SM signal to the Analyze Board goes high which puts its shift registers into the shift mode. Counts one through eight are what is known as the analyze time. During these counts, the stochastic arithmetic is going on and the normalized profile is being stored or compared on the memory boards.

During count nine the Result Analyzer Board is active and a NAND gate from the counter sends a signal to this board telling it to get to work. This completes one time frame. Note that it is the analysis of one angular view only.

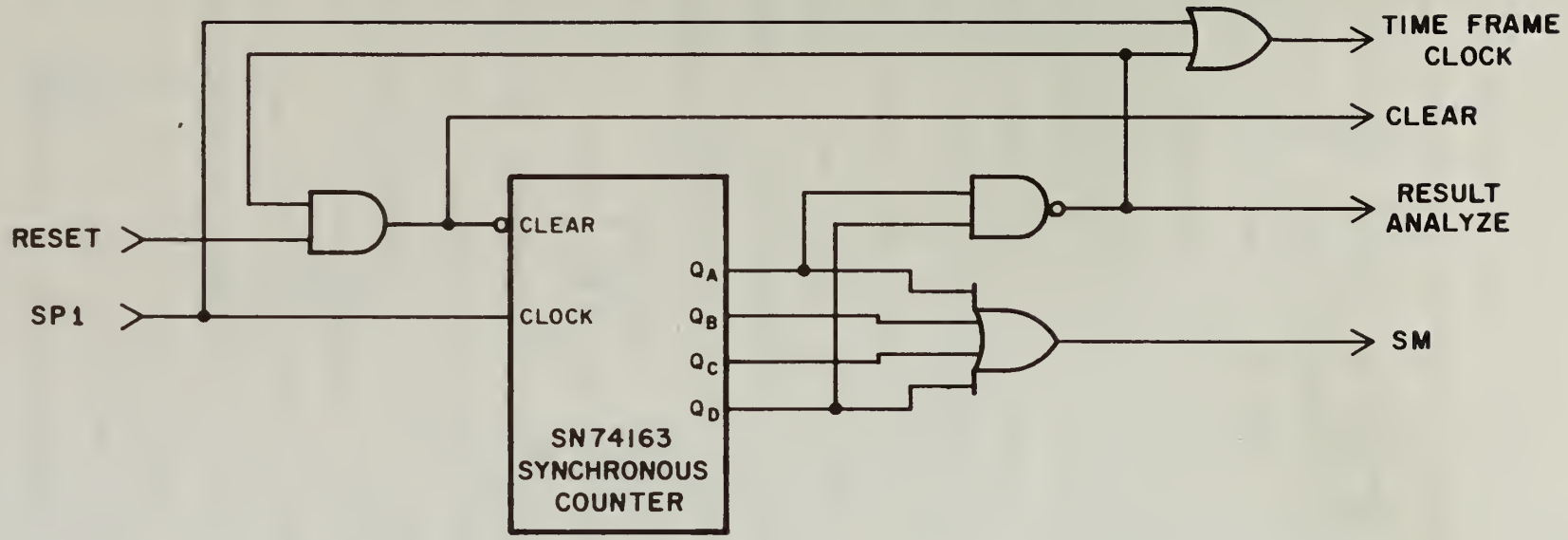


Figure 4.14 Time Frame Generator Portion of Control Board

4.12.2 Time Frame Counter

Since eighteen angles must be looked at to take care of rotation, the procedure mentioned above must be gone through eighteen times. This section (Figure 4.15) consists essentially of a counter which counts the time frames and drives a demultiplexer with nineteen outputs. The first eighteen outputs each go to an Input Board to activate one particular angular view during a time frame. In the analyze mode eighteen time frames are completed and on the nineteenth a signal called "THE END" goes low. This shuts off all activity including the main counter which generates the time frames and also initiates the display. The machine will stay in this nineteenth state until the ACTUATE switch is pushed and the whole cycle is started again.

In the store mode only one angular view is stored, therefore there is no need to go through eighteen time frames: Only one is needed. However because of the structure of the memory boards, no output for display is possible in a store cycle. Since it would be nice to get a display of the total number of counts in the profile buffers just to make sure they are working, this section of the Control Board makes display possible in a unique way. When the machine is in the sotre mode, which simply means that one MBN line is being pulled low, one time frame is gone through in the usual manner with one memory location storing the profile information. Then a second time frame is run through with the MBN signal being released. This means that all the memory boards are now doing an analyze cycle in which the absolute difference is found between the profile stored and the incoming profile. If the incoming profile pulses are shut off, as they are by the SRPS--BLANK signal, the number in the fit buffer will be the total number of counts in the stored profile. The machine then enters a third time frame, THE END goes low as before and the number being displayed

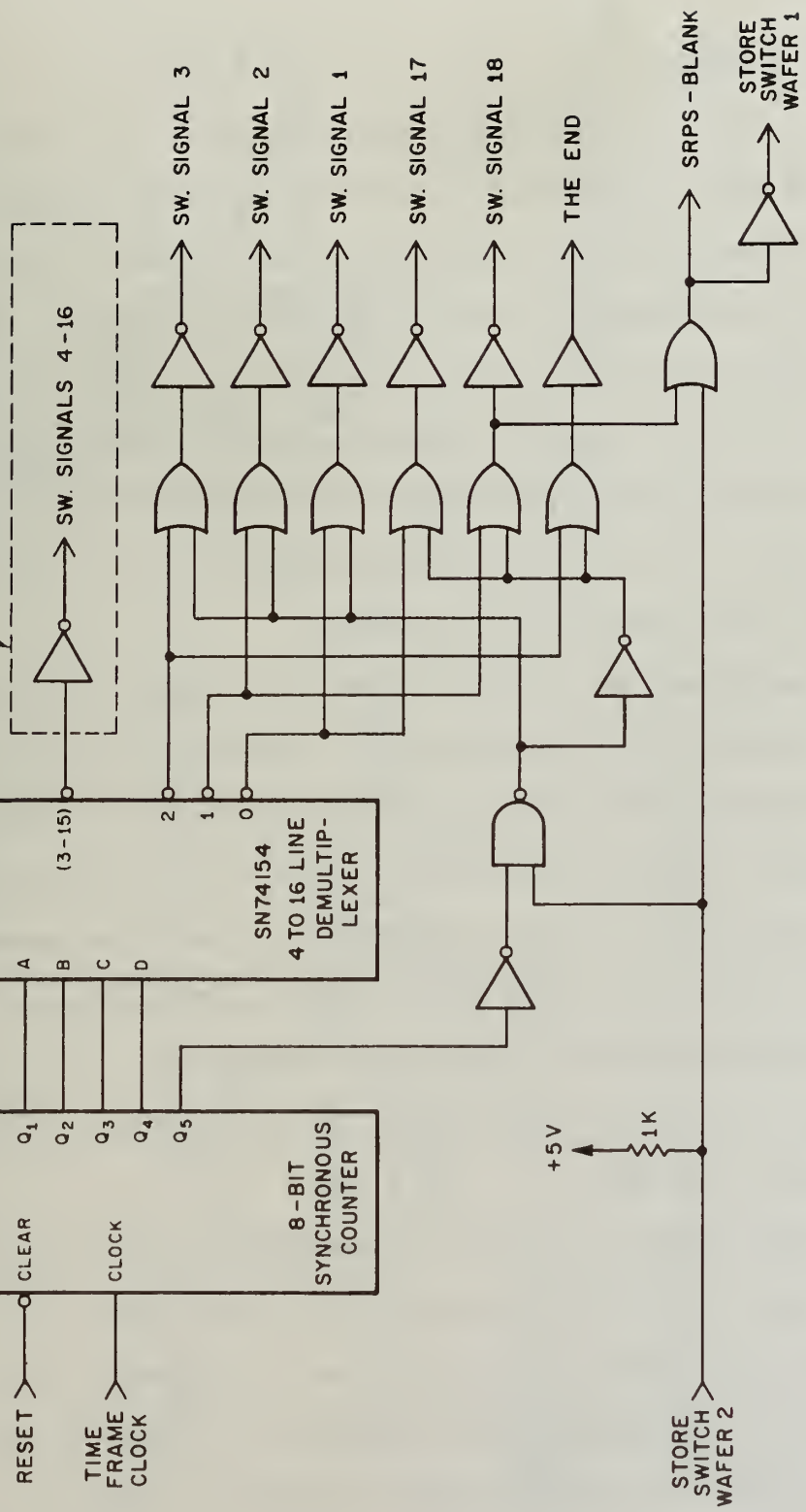


Figure 4.15 Time Frame Counter Portion of Control Board

will be the total number of counts in the profile buffer of the memory location selected.

4.12.3 GSV Generator

This section of the Control Board (Figure 4.16) is active only during the analyze time of the time frame. Its purpose is to provide the differing rates of gradual switching values used by the Stochastic Arithmetic Board as determined by the Number of Active Lines (NAL) information. It consists of a demultiplexer with sixteen outputs, one of which is driven low by the NAL number. An array of OR gates on the outputs of the demultiplexer is used to select which switching point signal from the ROM will get through to drive a counter. The counter is set up to count to seven, reset itself to zero, and continue counting in this manner.

To understand how this gradual switching scheme works, take the example of having only two lines active. This means that only the first two shift registers of the Analysis Board have non-zero information. The switching point signal chosen and let through to the counter will be SP 1. Since SP 1 also drives the main counter of the time frame generator and the analyze time is eight SP 1 pulses long, the GSV counter will only have a chance to count from zero to seven in the analyze time. We recall from the discussion of the SRPS Arithmetic Board how this gradually switches from one register to the next.

If three lines are active, the counter has a chance to count from zero to seven, reset itself, and count up to seven again. At the reset point, four small SHIFT pulses are sent out to the Analyze Board to shift the contents of each shift register up from one register to the next. In this manner each unnormalized profile is expanded in time.

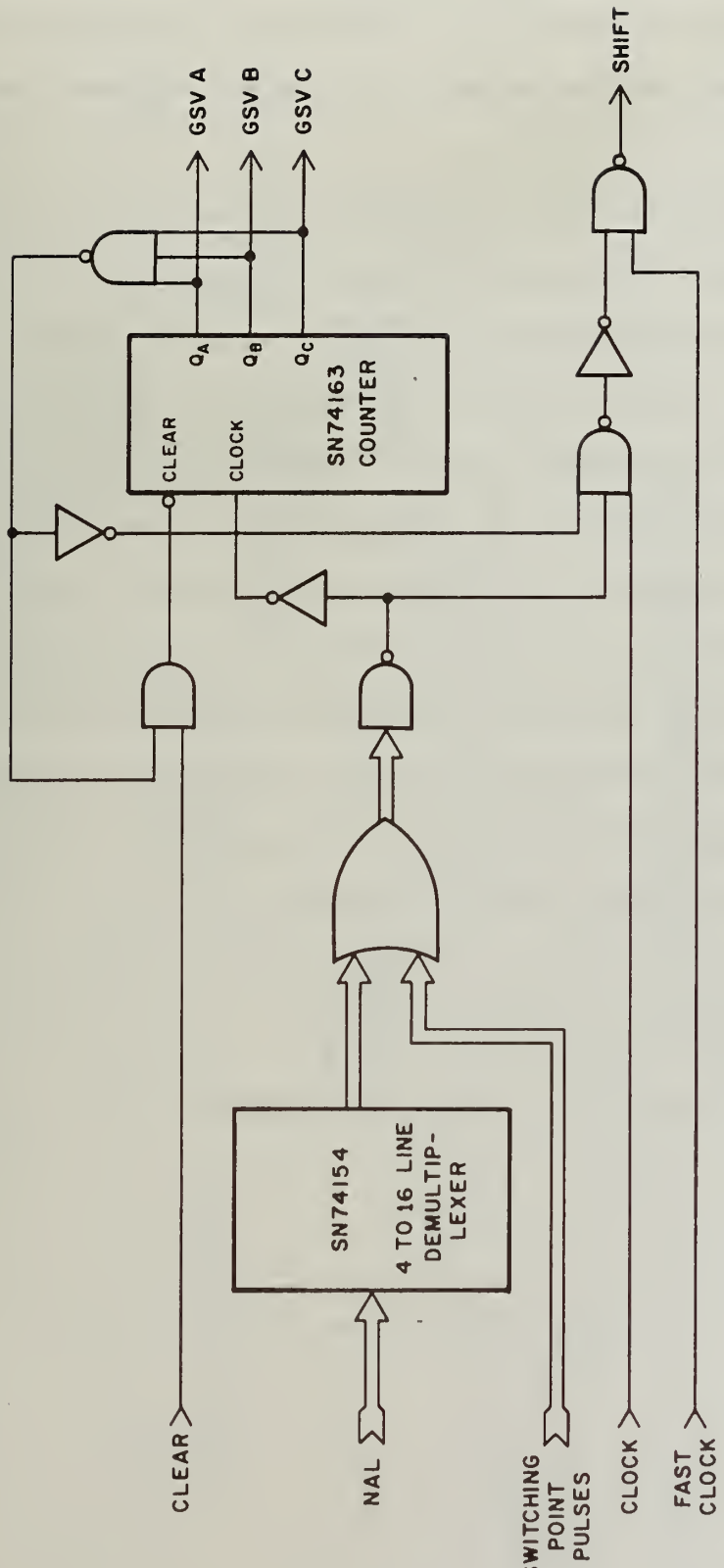


Figure 4.16 GSV Generator Portion of Control Board

4.12.4 Memory Address Generator

This section (Figure 4.17) is also active only during the analyze time. Its job is to generate the specialized pulses and addresses required by the memory boards.

The analyze time has to be divided into eleven discrete periods for the memory boards. This section contains a two piece counter driven by SP 11. The first section of the counter scales SP 11 by eight to take care of the fact that the analyze time is eight SP 1 pulses long. When this first section does emit a pulse, it sends it to a shift register operating on a fast clock in the shift right mode. The pulse travels through the shift register from the Q_A output to the Q_D output. As the pulse travels past the Q_A output it is seen by the memory boards as an MCP 1 pulse. The Q_B output increments the counter containing the memory address. At Q_D the pulse emits an MCP 2 to the memory boards. This series of events happens eleven times during the analyze period ensuring that all eleven registers of the profile buffer are filled or analyzed.

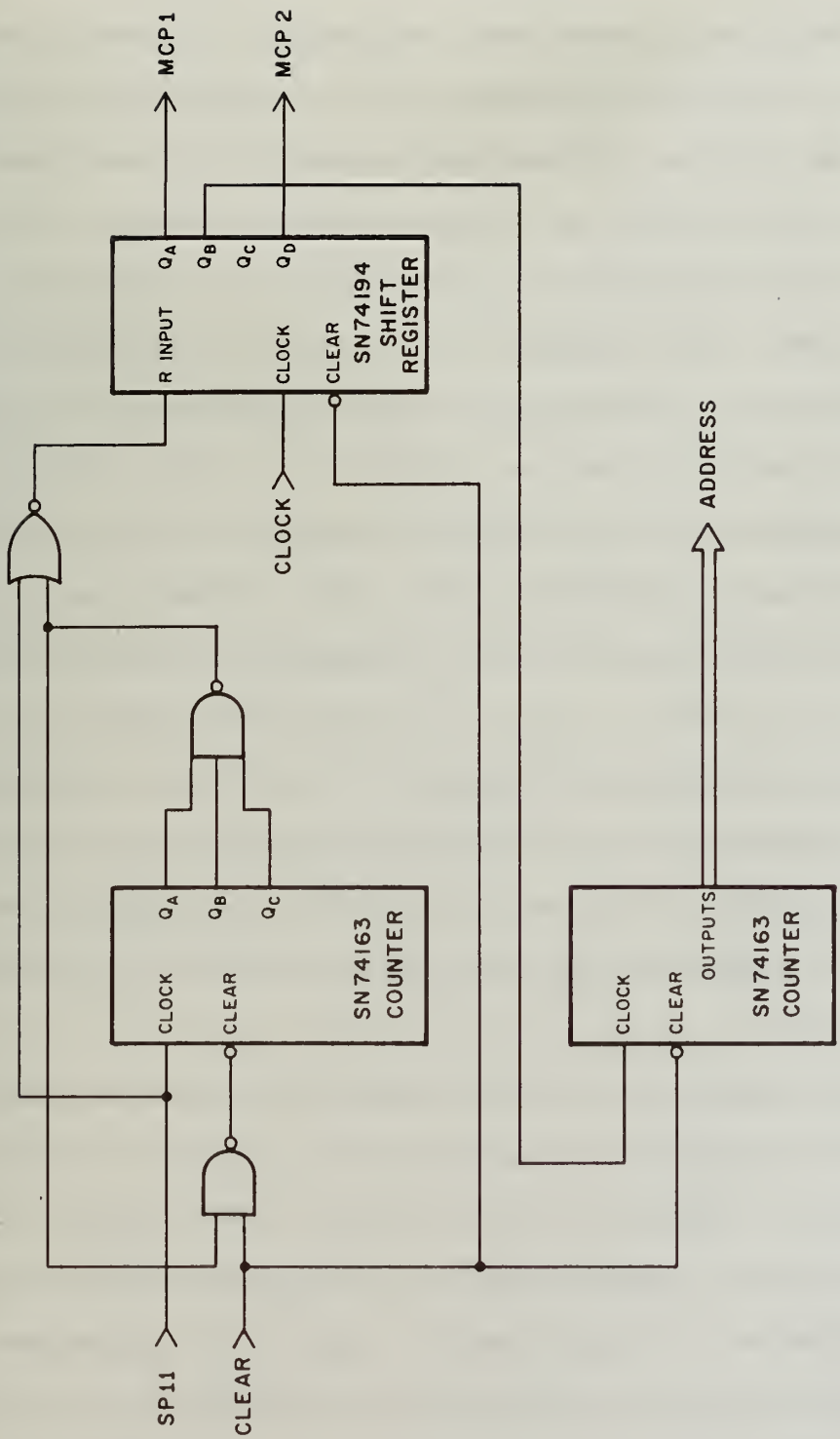


Figure 4.17 Memory Address Generator Portion of Control Board

5.0 CONCLUSION

NORMAN clearly demonstrates the viability and power of the type of "intelligent scanning" and stochastic (i.e. probabilistic) processing employed in the machine. The main limiting factors to the machine, as it now exists, is its resolution and storage capability. NORMAN is able to recognize most of the figures in its library without much difficulty. Any mistakes that it does occasionally make appear to be independent of the size, position, and rotation of the figure. The mistakes occur between such closely matching figures as a HEXAGON and a CIRCLE and can be attributed to the resolution of the input array. An interesting mistake which also sometimes occurs is that NORMAN calls a RING a RECTANGLE and vice-versa. This appears quite surprising until one remembers how NORMAN "sees" a RING. It does not see a RING as having a large hole in the center: i.e. it flattens the two sides of the RING together. The profile of a RING then appears exactly the same as that of a RECTANGLE, only with slightly rounded corners. In the rest of this chapter we shall describe changes that we feel would be necessary to make NORMAN into a more powerful machine, i.e. one that could read type, etc.

First of all, a more powerful machine would need more input resolution. A matrix of discrete phototransistors simply does not provide much resolution. One might want to think in terms of an integrated array with up to 10^6 elements. Another solution is a system in which the figure is scanned crosswise, such as a television camera. It is quite easy to imagine how one would build up a profile with a scanning system: a counter could be gated on by the black areas of the figure as it is scanned. The main problem with a scanning arrangement is that the scans must occur at different

angles to take care of revolution of the figure. Some sort of scheme would have to be worked out to either rotate the image or the scanning action.

Resolution is also limited by the size of the whole machine. The profile buffer would certainly have to be more than eleven registers wide. Also, although processing by means of SRPS signals with a 10 MHz clockrate is ideal in the present system, the analyze time might be too great in a larger machine since to get increased accuracy (resolution) with an SRPS signal requires a longer time interval to integrate over. Either a higher clock-rate would have to be chosen, or more operations would have to be done in parallel.

Lastly, more than one angular view of a figure should be stored. Figure 5.1 shows two separate figures whose profiles at a particular angle are the same. Clearly, the more views of a figure can be stored, the more resolution the machine will allow.

Just one final word about the recognition capabilities of NORMAN or any other larger hypothetical machine built around these principles. The recognition capability depends entirely on the shape of the figure and is independent of any pre-conceived notions regarding the figure. It would be interesting to integrate the ideas of this machine with other pattern recognition schemes currently being investigated which do require some knowledge of a figure. For instance, in a scanning type of arrangement it would not be too hard to detect "holes" in figures. This capability combined with the knowledge that the number "8", for example, must contain two holes, would permit recognition under more adverse conditions. Perhaps this could be extended so that NORMAN could read handwritten letters of arbitrary sizes and styles.

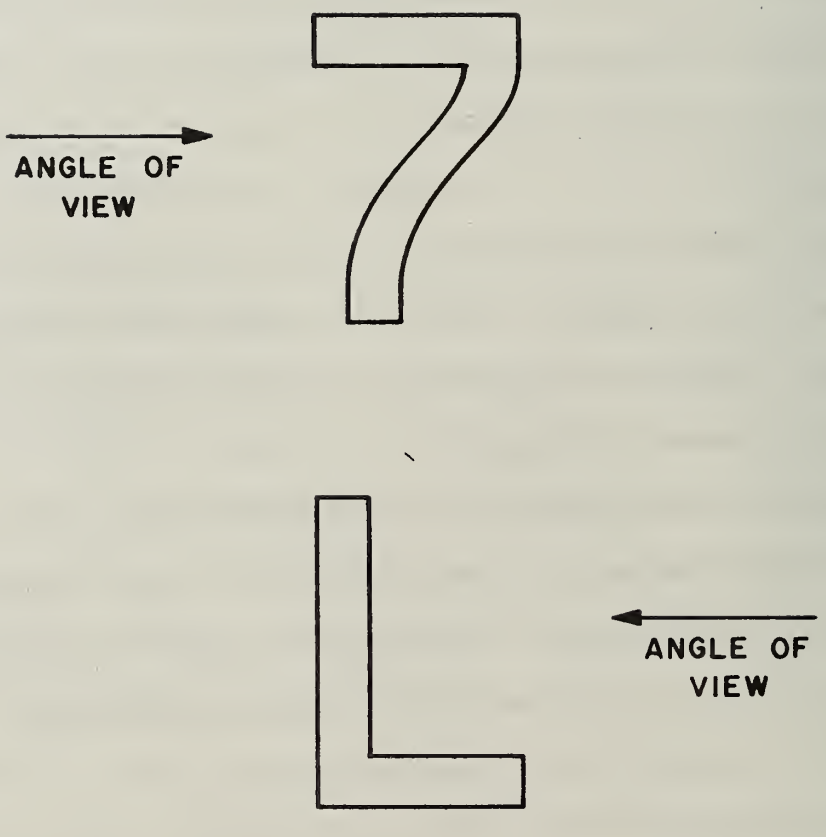


Figure 5.1 Two Figures which Present Exactly the Same Profile with the Above Angles of View

LIST OF REFERENCES

1. Afuso, C., "Analog Computation with Random Pulse Sequences," Department of Computer Science Report No. 255, University of Illinois, Urbana, Illinois, February 1968.

2. Ash, R. B., Information Theory, Wiley and Sons, New York, 1965.

3. Esch, J. W., "RASCEL - A Programmable Analog Computer Based on a Regular Array of Stochastic Computing Element Logic," Department of Computer Science Report No. 332, University of Illinois, Urbana, Illinois, June 1969.

4. Huberts, G., "Quarterly Technical Progress Report," Section 2.9, Department of Computer Science, University of Illinois, Urbana, Illinois, April, May, June 1973.

5. Huberts, G., "Quarterly Technical Progress Report," Section 1.3, Department of Computer Science, University of Illinois, Urbana, Illinois, October, November, December 1973.

6. Huberts, G., "Quarterly Technical Progress Report," Section 1.1, Department of Computer Science, University of Illinois, Urbana, Illinois, January, February, March 1974.

7. Peatman, J. B., The Design of Digital Systems, McGraw-Hill, New York, 1972.

8. Peterson, W. W., Error-Correcting Codes, MIT Press, Cambridge and Wiley and Sons, New York, 1961.

9. Poppelbaum, W. J., Computer Hardware Theory, Macmillan, New York, 1972.

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: UIUCDCS-R-75-715	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE *(and Subtitle)*: NORMAN (NORMalizing ANalyzer)	5. TYPE OF REPORT & PERIOD COVERED: M.S. Thesis
6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s): GARLAN JAN HUBERTS	8. CONTRACT OR GRANT NUMBER(s): N000-14-67-A-0305-0024
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Department of Computer Science, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: Office of Naval Research, 219 South Dearborn Street, Chicago, Illinois 60604	12. REPORT DATE: April 1975
	13. NUMBER OF PAGES: 64
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*	15. SECURITY CLASS. *(of this report)*
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Input array
Intelligent scanning
Normalized profile
Stochastic processing

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

NORMAN is a pattern recognition machine which recognizes two-dimensional figures under conditions of translation, rotation, and magnification. It uses "intelligent scanning" to build up a profile of any arbitrary figure and stochastic (i.e. probabilistic) processing to normalize the profile with respect to the three permutations.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601 |

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

BIBLIOGRAPHIC DATA SHEET	1. Report No. UIUCDCS-R-75-715	2.	3. Recipient's Accession No.
4. Title and Subtitle NORMAN (NORMalizing ANalyzer)			5. Report Date April 1975 6.
7. Author(s) GARLAN JAY HUBERTS			8. Performing Organization Rept. No. UIUCDCS-R-75-715
9. Performing Organization Name and Address Department of Computer Science University of Illinois at Urbana-Champaign Urbana, Illinois 61801			10. Project/Task/Work Unit No. 11. Contract/Grant No. N000-14-67-A-0305-0024
12. Sponsoring Organization Name and Address Office of Naval Research 219 South Dearborn Street Chicago, Illinois 60604			13. Type of Report & Period Covered M.S. Thesis 14.

15. Supplementary Notes

16. Abstracts

NORMAN is a pattern recognition machine which recognizes two-dimensional figures under conditions of translation, rotation, and magnification. It uses "intelligent scanning" to build up a profile of any arbitrary figure and stochastic (i.e. probabilistic) processing to normalize the profile with respect to the three permutations.

17. Key Words and Document Analysis. 17a. Descriptors

Input array
Intelligent scanning
Normalized profile
Stochastic processing

17b. Identifiers/Open-Ended Terms

17c. COSATI Field/Group

18. Availability Statement	19. Security Class (This Report)	21. No. of Pages
unlimited distribution	UNCLASSIFIED	64
	20. Security Class (This Page) UNCLASSIFIED	22. Price

USCOMM-DC 40329-P71

BIBLIOGRAPHIC DATA SHEET	1. Report No. UIUCDCS-R-75-715	2.	3. Recipient's Accession No.
4. Title and Subtitle NORMAN (NORMalizing ANalyzer)			5. Report Date April 1975 6.
7. Author(s) GARLAN JAY HUBERTS			8. Performing Organization Rept. No. UIUCDCS-R-75-715
9. Performing Organization Name and Address Department of Computer Science University of Illinois at Urbana-Champaign Urbana, Illinois 61801			10. Project/Task/Work Unit No. 11. Contract/Grant No. N000-14-67-A-0305-0024
12. Sponsoring Organization Name and Address Office of Naval Research 219 South Dearborn Street Chicago, Illinois 60604			13. Type of Report & Period Covered M.S. Thesis 14.

15. Supplementary Notes

16. Abstracts

NORMAN is a pattern recognition machine which recognizes two-dimensional figures under conditions of translation, rotation, and magnification. It uses "intelligent scanning" to build up a profile of any arbitrary figure and stochastic (i.e. probabilistic) processing to normalize the profile with respect to the three permutations.

17. Key Words and Document Analysis. 17a. Descriptors

Input array
Intelligent scanning
Normalized profile
Stochastic processing

17b. Identifiers/Open-Ended Terms

17c. COSATI Field/Group

18. Availability Statement	19. Security Class (This Report)	21. No. of Pages
unlimited distribution	UNCLASSIFIED	64
	20. Security Class (This Page) UNCLASSIFIED	22. Price

USCOMM-DC 40329-P71

BIBLIOGRAPHIC DATA SHEET	1. Report No. UIUCDCS-R-75-715	2.	3. Recipient's Accession No.

4. Title and Subtitle

NORMAN (NORMalizing ANalyzer)

5. Report Date: April 1975

6.

7. Author(s)

GARLAN JAY HUBERTS

8. Performing Organization Rept. No. UIUCDCS-R-75-715

9. Performing Organization Name and Address

Department of Computer Science
University of Illinois at Urbana-Champaign
Urbana, Illinois 61801

10. Project/Task/Work Unit No.

11. Contract/Grant No. N000-14-67-A-0305-0024

12. Sponsoring Organization Name and Address

Office of Naval Research
219 South Dearborn Street
Chicago, Illinois 60604

13. Type of Report & Period Covered: M.S. Thesis

14.

15. Supplementary Notes

16. Abstracts

NORMAN is a pattern recognition machine which recognizes two-dimensional figures under conditions of translation, rotation, and magnification. It uses "intelligent scanning" to build up a profile of any arbitrary figure and stochastic (i.e. probabilistic) processing to normalize the profile with respect to the three permutations.

17. Key Words and Document Analysis. 17a. Descriptors

Input array
Intelligent scanning
Normalized profile
Stochastic processing

17b. Identifiers/Open-Ended Terms

17c. COSATI Field/Group

18. Availability Statement	19. Security Class (This Report)	21. No. of Pages
unlimited distribution	UNCLASSIFIED	64
	20. Security Class (This Page) UNCLASSIFIED	22. Price